Honeywell

620-0048 & 620-0052 Data Collection Modules User Manual

620-8980
Rev. C
06/92
Supersedes: 12/89

Copyright, Notices, and Trademarks

Revision C – June 1, 1992

This document was prepared using Information Mapping® methodologies and formatting principles.

Honeywell
Industrial Automation and Control
Automation College
1100 Virginia Drive
Fort Washington, PA 19034

(215) 641-3126

About This Publication

This publication provides comprehensive information, including protocol and instructions, for interfacing the Model 620-0048 or Model 620-0052 Data Collection Module (DCM) with a general purpose computer. Features and functions that differ between the two modules are described separately throughout the manual.

For applications in which a DCM is interfaced with a 627 MiniCOP microcomputer using Honeywell communications software, only the installation, configuration, and theory of operation sections (Sections 2, 3, and 4) of this manual apply. Other user information is contained in the user manual of the host device interfaced by the DCM.

This manual, Revision C, is intended for use with Revision 3.1 620-0048 firmware and Revision 2.0 620-0052 firmware.

Table of Contents

Figures and Tables

Continued on next page

Figures and Tables

Continued on next page

Continued on next page

Figures and Tables

Continued on next page

Acronyms

CPM ..... Control Processor Module
CRC ..... Cyclic Redundancy Check
CS, CTS ..... Clear-to-Send
DCD ..... Data Carrier Detect
DCE ..... Data Communications Equipment
DCM ..... Data Collection Module
DHP ..... Data Hiway Port
DSR ..... Data Set Ready
DTE ..... Data Terminal Equipment
DTR ..... Data Terminal Ready
EIA ..... Electronic Industries Association
EMI ..... Electromagnetic Interference
FCC ..... Federal Communications Commission
ICS ..... Institute of Computer Science
IEC ..... International Electrotechnical Commission
IEEE ..... Institute of Electrical and Electronics Engineers
I/O ..... Input/Output
ISO ..... International Standards Organization
LCS ..... Logic Controller System
LED ..... Light-Emitting Diode
NEMA ..... National Electrical Manufacturer's Association
PC ..... Personal Computer
RD ..... Receive Data
RFI ..... Radio Frequency Interference
RTS, RS ..... Request-To-Send
RXD ..... Receive Data
SD ..... Send Data
TXD ..... Transmit Data
VDE ..... Variable Display Equipment

ATTENTION

ATTENTION: Refer to the *Glossary* (at the back of this manual) for detailed definitions of the following terminology which are used throughout this manual:

- Clear to Send (CTS, CS)
- Data Carrier Detect (DCD, RR)
- Data Set Ready (DSR)
- Data Terminal Ready (DTR)
- Receive Data (RXD, RD)
- Request to Send (RTS, RS)
- Shield Ground
- Signal Ground
- Transmit Data (TXD, SD)

References

Publication Title	Publication Number	Binder Title	Binder Number
620-11/14/16 Logic Controller System User Manual	620-8976	620 System	VOLUME I
620-12/1633/36 Logic Controller System User Manual	620-8964	620 System	VOLUME II
620 Installation and 621 I/O Communications User Manual	620-8996	620 System	VOLUME I
620 Installation and 621 I/O Communications for 620-12/1633/36 Logic Controller Systems User Manual	620-8962	620 System	VOLUME II
621 I/O Specifications User Manual	620-8995	620 System	VOLUME II
623-60 MS-DOS Loader User Manual	620-8983	620 System	VOLUME VI
623-6100/6150 Loader/Terminal User Manual	623-8940	620 System	VOLUME VI

Section 1 – Data Collection Modules (DCMs)

Overview

Section contents

Function of the 620-0048 & 620-0052 Data Collection Modules (DCM)

The 620-0048 and 620-0052 Data Collection Modules (DCMs) are communication interface modules used to connect 620 Logic Controller Systems (LCSs) with general purpose computers.

- The 620-0048 DCM contains one serial interface port that supports data collection.
- The 620-0052 DCM contains two ports:
  - port 1 performs data collection functions or general purpose communications interface functions, and
  - port 2 performs general communications interface functions.

Continued on next page

620-0048 & 620-0052 DCM features

Features of the 620-0048 and 620-0052 DCMs are listed below.

- Both DCMs can be used as general purpose communication interface modules for 620 Logic Controller Systems (LCSs). Any 620 LCS user program memory contents, input/output status, data registers, or system register contents may be examined or modified through the DCM. The DCM provides this access for other services beyond the capabilities of the programmable controller.
- Each DCM provides low- to medium-speed connection of a 620 LCS to another computing device. Each port implements Honeywell's asychronous byte count (ABC) protocol, which provides a simple, easy-to-implement interface to any 620 LCS. The ABC protocol is suitable for use in both point-to-point and multidrop network applications. Data transparency is achieved through a byte count procedure that eliminates the need for a special data encoding for character insertion and deletion.
- Each DCM port can operate as a front-end communication processor to the 620 LCS. In this capacity each port performs computer interface functions between a host computer and the 620 LCS. Both ports on the 620-0052 can be used for communication interface, thereby providing the functionality of two communications interfaces within a single module width.
- The serial ports of both DCMs are capable of asynchronous data transmission. Internal timing generation provides communication at standard I/O rates of 110, 300, 600, 1200, 2400, 4800, 9600, and 19.2K baud.
- Each DCM port interfaces to a host device in conformance to the electrical characteristics of EIA Standards RS232 and RS422/RS485. The electrical interface is capable of either half- or full-duplex circuit operation.
- Point-to-point wiring is possible with each type of electrical interface. Multipoint operation is possible in these cases:
  - RS232 interface and modem suitable for multipoint operation are used.
  - RS422/RS485 interface is used with or without a modem.

Continued on next page

620-0048 and 620-0052 DCM specifications

Refer to Table 1-1 for general specifications for the 620-0048 and 620-0052 DCMs.

Table 1-1 620-0048 and 620-0052 DCM Specifications

Item	Specification
Operating Temperature	0°C to 60°C (32°F to 140°F)
Storage Temperature	-40°C to 85°C (-40°F to 185°F)
Humidity	0 to 95% (noncondensing)
Dimensions	26.7 x 3.05 x 16.51 cm (10.5 x 1.2 x 6.5 inches)
Weight	0.49 kg (1.1 lbs)
IEC 68-2-6 Test FC Frequency Range	10 to 150 Hz
Vibration Amplitude	0.006 inches (0.15 mm) peak-to-peak from 10 to 57 Hz, 1 G constant acceleration from 57 to 150 Hz
Showering Arc Test	NEMA-ICS-1-109
FCC Rulings on Emitted RFI	Docket #20780 Part #15
IEEE Surge Withstand Standard	#587-1080
Honeywell Noise Test	VDE-0871 Class A

Continued on next page

Power supply loading

Refer to Table 1-2 for the power supply consumption for the 620-0048 DCM and Table 1-3 for the power supply consumption for the 620-0052 DCM.

Table 1-2 620-0048 Power Consumption

620-0048 POWER SUPPLY		I (TYPICAL)	I (MAXIMUM)
5V		1.3A	1.5A
+12V -12V	620-20/25 620-30/35	60mA	100mA
+15V -15V	620-06/10/15 620-11/14/16	60mA	100mA
	620-12 620-1633 620-36	60mA	100mA

Table 1-3 620-0052 Power Consumption

620-0052 POWER SUPPLY		I (TYPICAL)	I (MAXIMUM)
5V		1.6A	1.8A
+12V -12V	620-20/25 620-30/35	74mA	90mA
+15V -15V	620-06/10/15 620-11/14/16	74mA	90mA
	620-12 620-1633 620-36	74mA	90mA

Continued on next page

RS232 electrical specifications

All signals compatible to RS232 adhere to EIA RS232C standard (Section 2 – *Electrical Signal Characterisitics*) specifications.

RS422/RS485 electrical specifications

All signals compatible to RS422A/RS485 adhere to EIA RS422A/RS485 standard spcifications. The following additional specifications apply to support multidrop operation:

- common mode output voltage line drivers: -7V, +12V,
- tristate control through RTS (RS) on SD line driver,
- thermal shutdown protection on line drivers,
- positive and negative current limiting (line drivers),
- input impedance of line receivers: 12K ohms minimum, and
- 150-ohm line termination on RD, CS, RR receivers (RD selectable).

ATTENTION

ATTENTION: Refer to the *Glossary* (at the back of this manual) for detailed definitions of the following terminology which are used throughout this manual:

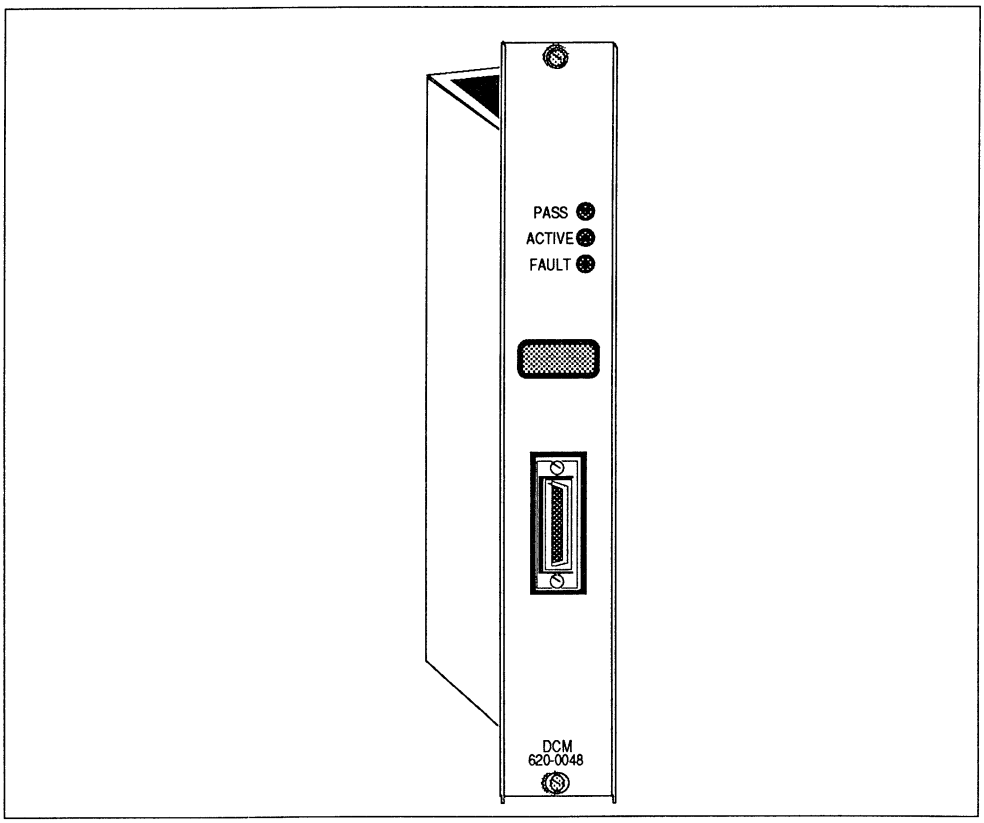
- Clear to Send (CTS, CS)
- Data Carrier Detect (DCD, RR)
- Data Set Ready (DSR)
- Data Terminal Ready (DTR)
- Receive Data (RXD, RD)
- Request to Send (RTS, RS)
- Shield Ground
- Signal Ground
- Transmit Data (TXD, SD)

DCM Functional Description

DCM frontplate

Figure 1-1 shows the frontplate of the 620-0048 DCM and Figure 1-2 shows the frontplate of the 620-0052 DCM.

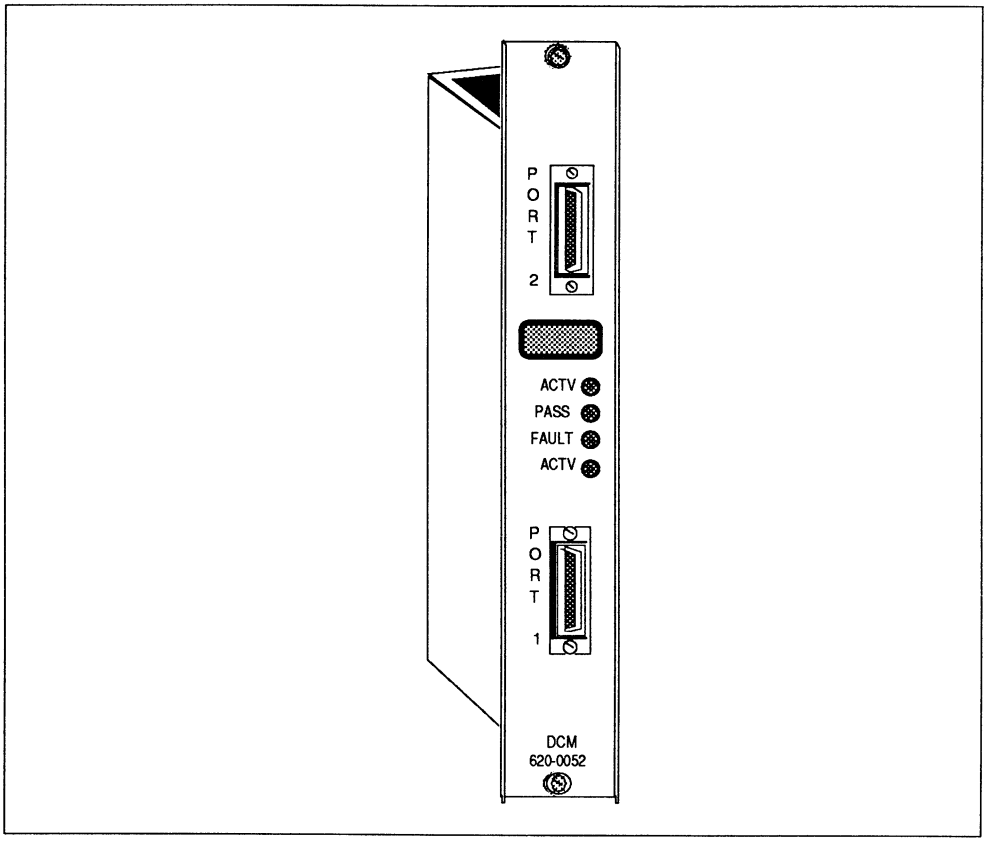
Figure 1-1 620-0048 DCM Frontplate



Continued on next page

DCM frontplate, continued

Figure 1-2 620-0052 DCM Frontplate



Continued on next page

Indicators and connectors

The DCM frontplate indicators and connectors are used to view certain operating conditions and to set up the DCM for proper operation. There are three LED status indicators on the frontplate of the 620-0048 DCM and four status indicators on the frontplate of the 620-0052 DCM. Table 1-4 describes the indicators and connectors on the frontplate of each module

Table 1-4 DCM Indicators and Connectors

Indicator/Connector	Description
Status LEDs • PASS (green)	Lit when the module self-test is successfully completed at processor power-up.
• ACTIVE (green)	Lit during the reception and transmission of a message through the port.
• FAULT (red)	Lit prior to the DCM establishing communications with the 620 LCS and whenever the DCM loses communications with the 620 LCS. **ATTENTION** The FAULT LED also lights if the DCM fails its diagnostic test.
DTE Port(s)	25-pin D-series subminiature receptacle connectors (AMP HDP-20 series metal shell connectors equipped with an AMP 206512-1 locking post assembly) that serve as serial ports that are switch-selectable for either RS232 or RS422/RS485 compatibility.

Section 2 – DCM Installation

Overview

Section contents

Installation procedure

To install a DCM module, follow the general procedure outlined in Table 2-1.

Table 2-1 General Procedure for Installing DCM

Step	Action	Procedure Reference
1	Install network cabling.	*Network Installation* – see page 11.
2	Install DCM wiring.	*DCM Wiring* – see page 17.
3	Set appropriate DIP switches.	*Section 3 — DCM Configuration* — see page 27.
4	Install DCM in 620 LCS processor rack.	*Installing the DCM Module* — see page 10.

Installing the DCM Module

DCM option slot locations

The 620-0048 and 620-0052 DCMs are single-slot modules that must be placed in an appropriate option slot of a 620 LCS. Refer to Table 2-2 for the various processors and processor racks and the positions available for option modules.

Table 2-2 DCM Option Slot Locations

Processor	Processor Rack	Option Slots
620-06/10/15	620-0090/0091	M
620-11/14/1631	620-1690/1693	K or L
620-12/1633/36	620-1690/1693	K or L
	620-3691	I, J, K, or L
620-20/25	620-2590	A or B
620-30/35	620-3590	A, B, C, or D

ATTENTION

ATTENTION: Before installing the DCM in the 620 LCS processor rack, make sure that:

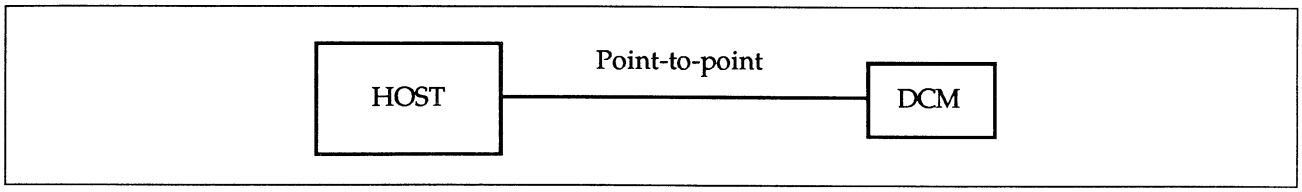
- network cabling is properly installed (refer to *Network Installation*);
- DCM wiring is properly installed and ready to be connected to the DCM communications port (refer to *DCM Wiring*); and
- DCM DIP switches have been properly set (refer to *Section 3 - DCM Configuration*).

Network Installation

DCM configurations

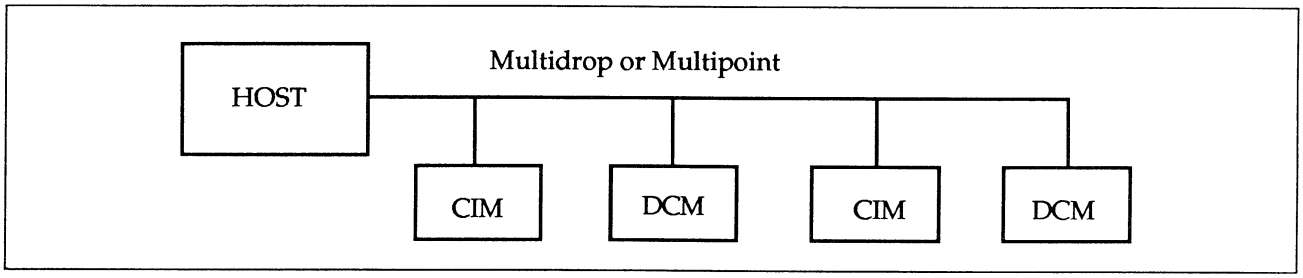
There are two types of configurations for interconnecting DCM(s) to a host. A point-to-point connection is between only two points (see Figure 2-1).

Figure 2-1 Point-to-Point Configuration



A multipoint/multidrop configuration connects three or more points on a common line; there is a single master and series of slaves (see Figure 2-2).

Figure 2-2 Multipoint/Multidrop Configuration



Twisted-pair networking

The DCM is designed with an RS422/RS485 multidrop compatible serial port, therefore it is possible to configure a multidrop network without modems. Refer to Table 2-3 for RS422/RS485 multidrop network specifications.

Table 2-3 RS422/RS485 Multidrop Network Specifications

Item	Specification
Maximum Population	32 DCM port connections per network trunk
Maximum Trunk Length	Cable dependent
Maximum Branch Length	61 cm (2 feet)
Data Rate	110, 300, 600, 1200, 2400, 4800, 9600, and 19.2K baud

Continued on next page

Twisted-pair network topology

The twisted-pair network topology accommodates a maximum of thirty-two, two-foot branches extending from the network trunk to the DCM. The branches may be located at any point along the network trunk without restrictions on distance between branches.

Multidrop networking of DCMs to a host can be implemented with either single or two-twisted pair cable.

- Refer to Figure 2-8 (in *DCM Wiring Diagrams*) for the basic single twisted-pair topology. The network trunk consists of a single twisted-pair cable. The cable serves as an output line for host transmissions to the DCMs and as an input line for DCM response transmissions to the host.

- Refer to Figure 2-9 (in *DCM Wiring Diagrams*) for the basic two twisted-pair network topology. The network trunk consists of two twisted-pair cables. Trunk T serves as an output line for host transmission to the DCMs and Trunk R serves as an input line for DCM response transmissions to the host.

Continued on next page

RS422 multidrop connection

The RS422/RS485 serial interface is designed to be attached to the trunk line of a multidrop twisted-pair network. The network trunk may be either a single twisted-pair network or a two-twisted pair cable. Operating a single twisted-pair network rather than a point-to-point requires the following:

1. The host Send Data (SD) line driver must be configured to switch into the tristate mode when its serial interface is not in the transmit mode. To do this, connect the tristate control of the SD line driver to the Request to Send signal. Refer to Figure 3-2 (in Section 3) for an example circuit diagram as implemented by the DCM.

2. The Receive Data (RD) line receiver must have its termination resistor switch open except at the ends of a multidrop trunk line. In the point-to-point mode, the RD receiver is one end of a line, therefore the termination resistor switch must be closed. Refer to Figure 3-3 for the location of the termination resistor.

The connection of the RS422/RS485 interface to a modem (DCE) which operates on a multidrop network is actually a point-to-point connection from the DTE standpoint. The line configuration switch (SW1, switch 1 for 620-0048 DCMs; SW2 switch 7 for 620-0052 DCMs port 1; and SW4 switch 7 for 620-0052 DCMs port 2 — refer to Section 3 for specific details on setting DCM DIP switches) should be set for multidrop, so that the DCM operates in a half-duplex mode.

Continued on next page

DCM pin assignments and reference designators

Refer to Table 2-4 for DCM pin assignments and reference designators.

Table 2-4 DCM Pin Assignments and Reference Designators

Pin Number	Signal (I/O Description)	Connector Designator	Interface Type
1	Shield	--	
2	Transmit Data (Output)	TXD	RS232
3	Receive Data (Input)	RXD	RS232
4	Request to Send (Output)	RTS	RS232
5	Clear to Send (Input)	CTS	RS232
6	Data Set Ready (Input)	DSR	RS232
7	Signal Ground		
8	Data Carrier Detect (Input)	DCD	RS232
9	Not used		
10	-12V through 1K	-12V	RS232
11	Not used		
12	Request to Send (Output)	RS-A	RS422/RS485
13	Request to Send, Inv.	RS-B	RS422/RS485
14	Transmit Data, Inv. (Output)	SD-B	RS422/RS485
15	Transmit Data	SD-A	RS422/RS485
16	Clear to Send, Inv. (Input)	CS-B'	RS422/RS485
17	Clear to Send	CS-A'	RS422/RS485
18	Not used		
19	+12V through 1K	+12V	RS232/RS422/RS485
20	Data Terminal Ready (Output)	DTR	RS232
21	Receive Data, Inv. (Input)	RD-B'	RS422/RS485
22	Receive Data	RD-A'	RS422/RS485
23	Data Carrier Detect, Inv. (Input)	RR-B'	RS422/RS485
24	Data Carrier Detect	RR-A'	RS422/RS485
25	Not used		

Continued on next page

Network trunk cable

The network trunk cable must be routed past the 620 LCS. Branches from the network trunk connect the DCM to the trunk and are limited to 2 feet (0.6m) in length. The branch cable may be the same type as the trunk or a less rigid type of the same quality (for example, Belden 9182 for the network trunk and Belden 9729 for the branches).

Cable selection

When selecting data communications cable, observe the following guidelines:

1. Either two single twisted-pair cables or one two-pair cable must be used for two twisted-pair networks.
2. Individual shielding of each pair is recommended.
3. Characteristic cable impedance ≥ 100 ohms.
4. Network trunk must be properly terminated.
5. Construction that meets local building codes.

Continued on next page

Calculating network trunk length

The length of the network trunk is limited by the characteristics of the cable. Use the following equation to calculate the length of the network trunk for a specific cable.

Maximum Trunk Length (feet) = (Z/R) X 1000

where:

Z = Cable characteristic impedance (ohms)
R = Cable conductor resistance per 1000 feet (ohms)

Example: Belden 9182 cable

Z = 150 ohm
R = 14 ohms

Maximum Trunk Length = (150 ohms/14 ohms) X 1000 = 10,714 feet

Example: Belden 9729 cable

Z = 100 ohms
R = 24 ohms

Maximum Trunk Length = (100 ohms/24 ohms) X 1000 = 4166 feet

Network termination

Resistors must be attached at each end of each pair of the network trunk cable. Two resistors are required for single pair networks and four are required for two-pair networks. The resistor value must be equal to twice the characteristic impedance of the network trunk cable for the above equations to apply. The resistor power rating should be 1/8-watt or greater.

Example: Belden 9182 cable

Z = 150 ohms
Terminating resistors = 300 ohms

Cable identification

The network trunk may consist of one or two twisted-pair cables. Cable manufacturers color-code multipair cable to aid in the identification of conductors. Identify the cable conductors to network function before installation.

DCM Wiring

General considerations

Observe these considerations when installing the DCM:

- Maintain a 60°C (140 °F) or less ambient air temperature at the bottom of each 620 LCS rack assembly.
- Separate all 440VAC (or higher) electrical supply lines as far from 620 LCS components as is practical.
- Run all 440VAC lines in separate conduit from I/O wiring ducts.
- Separate AC and data wiring as far as is practical.
- Install all wiring according to IEEE Standard 518.
- Cross two cables carrying different types of signals (data versus power) at a right angle rather than running them parallel for any distance.
- Terminate all cables at both ends, excluding the shield. If a termination is not made or is intermittent, noise immunity is lost even though the system may transmit valid data.
- Ensure that the entire Communications Network System is grounded to earth ground. The maximum ground reference voltage is 5 volts.
- Shield continuity must be maintained. Ensure that shield leads are not broken.
- Route cables around rather than through high noise areas.
- Allow the minimum amount of unshielded wire that will accommodate connection.
- Route shielded data cable along grounded surfaces such as metal cabinet walls and in conduit or trays. Single shield cable is most effective when routed along grounded surfaces.
- Configurations implementing the RS232 interface require multiple connector cable rated for data transmission.

Continued on next page

General considerations, continued

- Configurations implementing RS422/RS485 interface require individually shielded twisted-pair cable with a characteristic impedance of 100 ohms or greater. Refer to Table 2-5 for recommended cables.

Table 2-5 Recommended Cables for DCM RS422/RS485 Operation

	Belden	Alpha
Single Twisted-Pair	9182	9823
Two Twisted-Pair	9729	—
Three Twisted-Pair	9730	6073

Continued on next page

Conduit shielding

Conduit or cable trays are used to route the network trunkline within the plant, for short distances or for several miles. Often the same conduit is used to carry both data and power wiring, creating a problem with electromagnetic interference. The choice of materials and configuration for the cable conduit can determine the degree of protection from this interference.

Refer to Table 2-6, which is taken from IEEE Standard 518 for the installation of electrical equipment, to compare different types of conduits and raceways for magnetic field attenuation at 60 Hz and for electrostatic attenuation at 100 KHz.

Table 2-6 Raceway Shielding

Raceway Shielding	Thickness mm (inches)	60 Hz Magnetic Field Attenuation Ratio	60 Hz Magnetic Field Attenuation dB	100 KHz Electrical Field Attenuation Ratio	100 KHz Electrical Field Attenuation dB
Free air		1:1	0	1:1	0
2-inch aluminum conduit	3.91 (.154)	1.5:1	3.3	2150:1	66.5
#16 gauge aluminum tray	1.52 (.060)	1.6:1	4.1	15500:1	83.9
#16 gauge aluminum tray	1.52 (.060)	3:1	9.4	20000:1	86.0
#16 gauge galv. ingot iron tray	1.52 (.060)	3.2:1	10.0	22000:1	86.8
2-inch IPS copper pipe	3.96 (.156)	3.3:1	10.2	10750:1	80.6
#16 gauge aluminum tray	1.52 (.060)	4.2:1	11.5	29000:1	89.3
#14 gauge aluminum tray	1.90 (.075)	6:1	15.5	23750:1	87.5
2-inch metallic tubing	1.65 (.065)	6.7:1	16.5	3350:1	70.5
2-inch rigid galv. conduit	3.91 (.154)	40:1	32.0	8850:1	78.9

Continued on next page

Cable spacing

As far as is practical, it is advised to separate noise-creating sources (such as those with time-varying voltage or time-varying current) from data signal cables. Group cables with similar levels of noise susceptibility together, and group those with similar levels of noise generation separately in trays and conduits.

IEEE defines the following four classes of wiring that differ in signal level and noise susceptibility:

- **Data 1** – high noise susceptibility; analog signals of less than 50V and digital signals of less than 15V.
- **Data 2** – medium susceptibility; analog signals greater than 50V and switching circuits.
- **Data 3** – low susceptibility; switching signals greater than 50V, analog signals greater than 50V, regulating signals of 50V with currents less than 20A; AC feeders less than 20A.
- **Power** – AC and DC buses of 0-1000V with currents of 20-800A.

Tray spacing

Refer to Table 2-7 for the recommended minimum distances between the top of one tray and the bottom of the tray above, or between sides of adjacent trays. Table 2-7 also lists the recommended distances between trays and conduits.

Table 2-7 Tray and Conduit Spacing

Cable Class	Tray Spacing cm (inches)	Tray-Conduit Spacing cm (inches)	Conduit Spacing cm (inches)
Data 1	0	0	0
Data 2	0	2.5 (1)	2.5 (1)
Data 3	15.2 (6)	10.1 (4)	7.6 (3)
Power	66.0 (26)	45.7 (18)	30.5 (12)

Continued on next page

Tray considerations

Refer to the following considerations when installing trays:

- When separate trays are impractical, Data 1 and 2 cables may be placed in the same tray, provided they are separated by a grounded steel barrier.
- Trays containing Data 1 and 2 cabling should have solid bottoms and tray covers to provide complete shielding.
- Ventilation slots or louvers may only be used in trays containing Data 3 cables.

Grounding

Adequate grounding is important for safety considerations and to reduce electromagnetic noise interference. A grounding path for the system components and enclosures should be provided. This ground is connected to the central ground for all electrical equipment and AC power within the user's facility (that is, earth ground). All earth ground connections must be permanent and provide a continuous low-impedance path to earth ground for induced noise currents and fault currents.

System ground is accomplished by the mounting hardware. A rack assembly grounding screw (optional) is provided with each chassis for customer use to connect the system components to earth ground. Local electrical codes must be observed when installing a DCM Network System. Refer to the *620 Installation and 621 I/O Communications User Manual*, the *620 Installation and 621 I/O Communications for 620-12/1633/36 Logic Controller Systems User Manual*, or the *620-12/1633/36 Logic Controller System User Manual*, as appropriate, for more information on grounding.

Continued on next page

DCM wiring diagrams

Refer to Figures 2-3 through 2-9 for network wiring information for all DCM configurations.

Figure 2-3 RS232 Connection to Full Function Modem

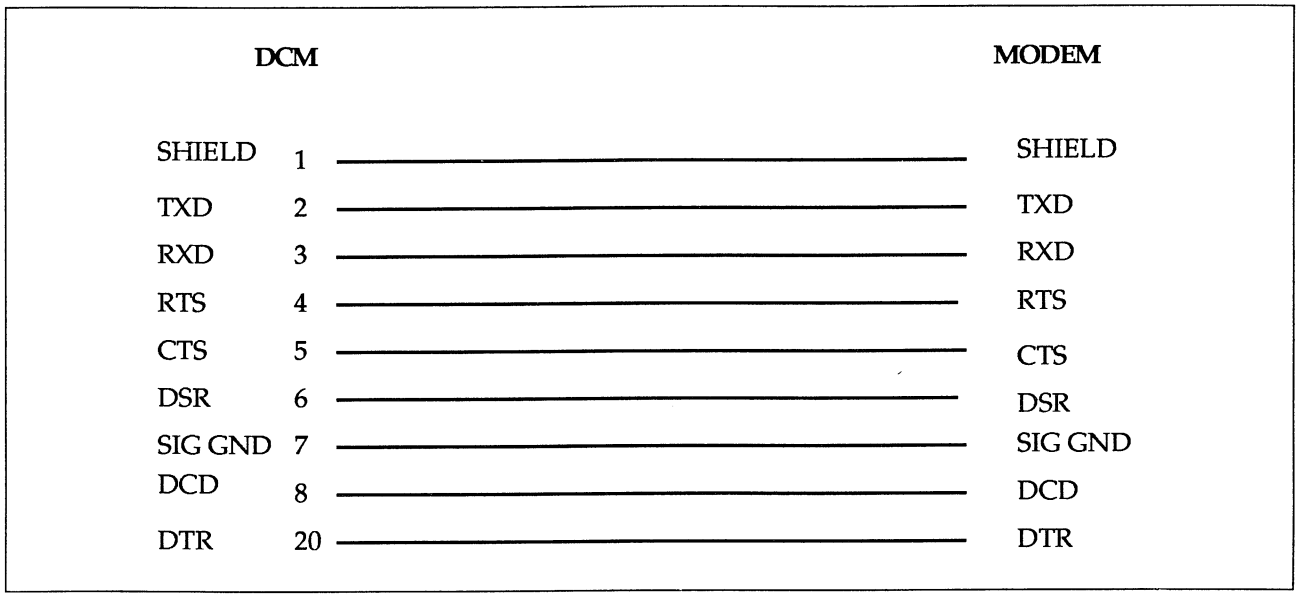
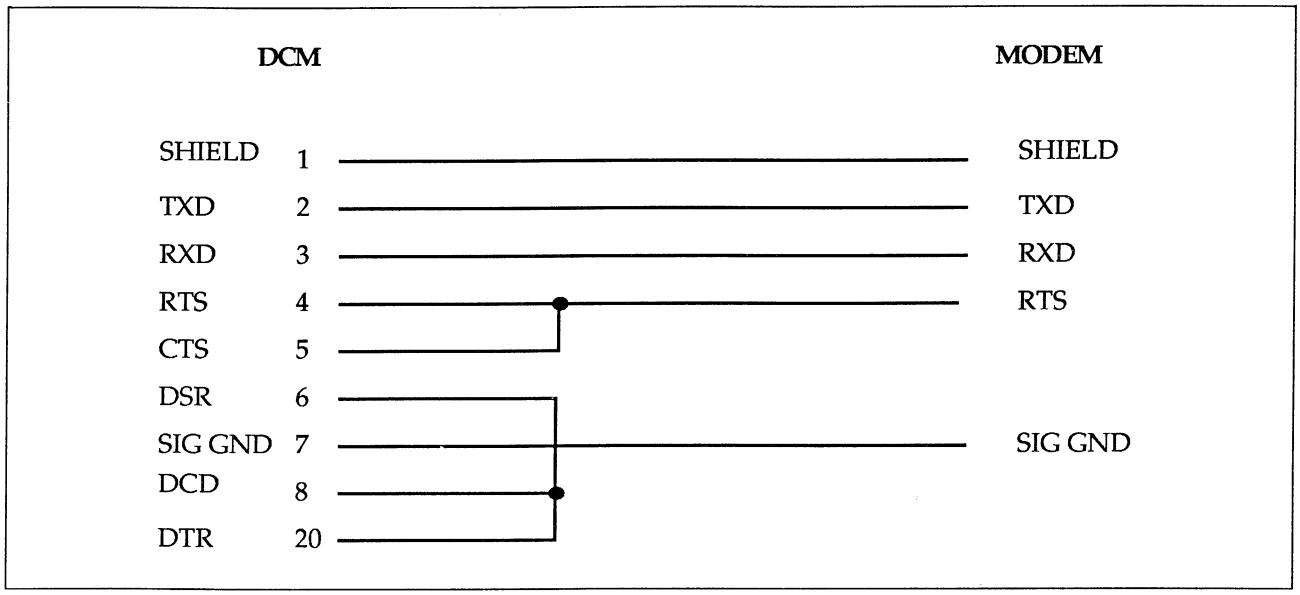


Figure 2-4 RS232 Connection to Minimum Function Modem



Continued on next page

DCM wiring diagrams,
continued

Figure 2-5 RS232 Connection to Host

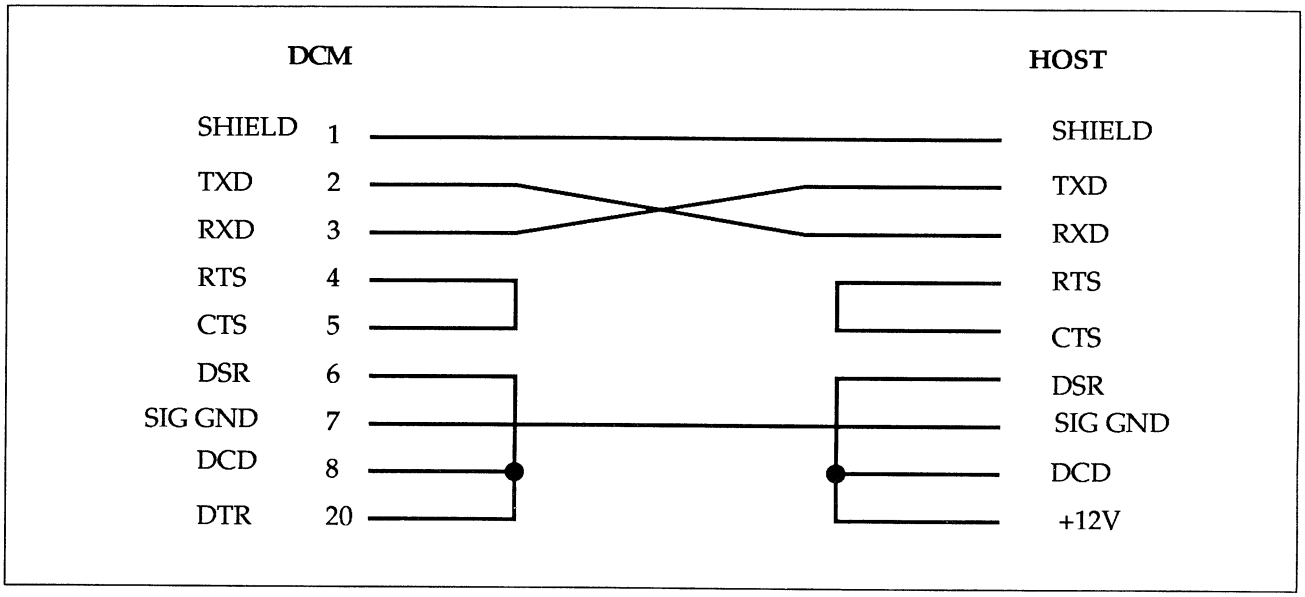
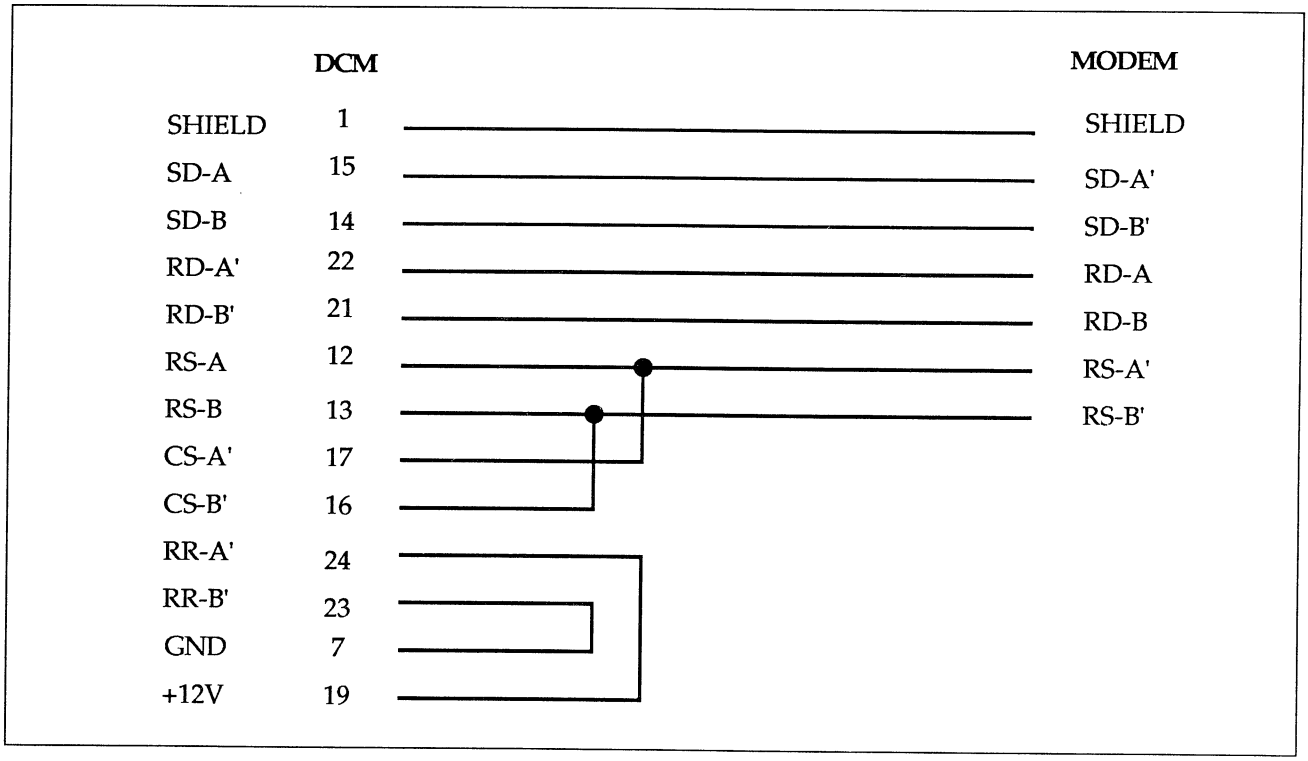


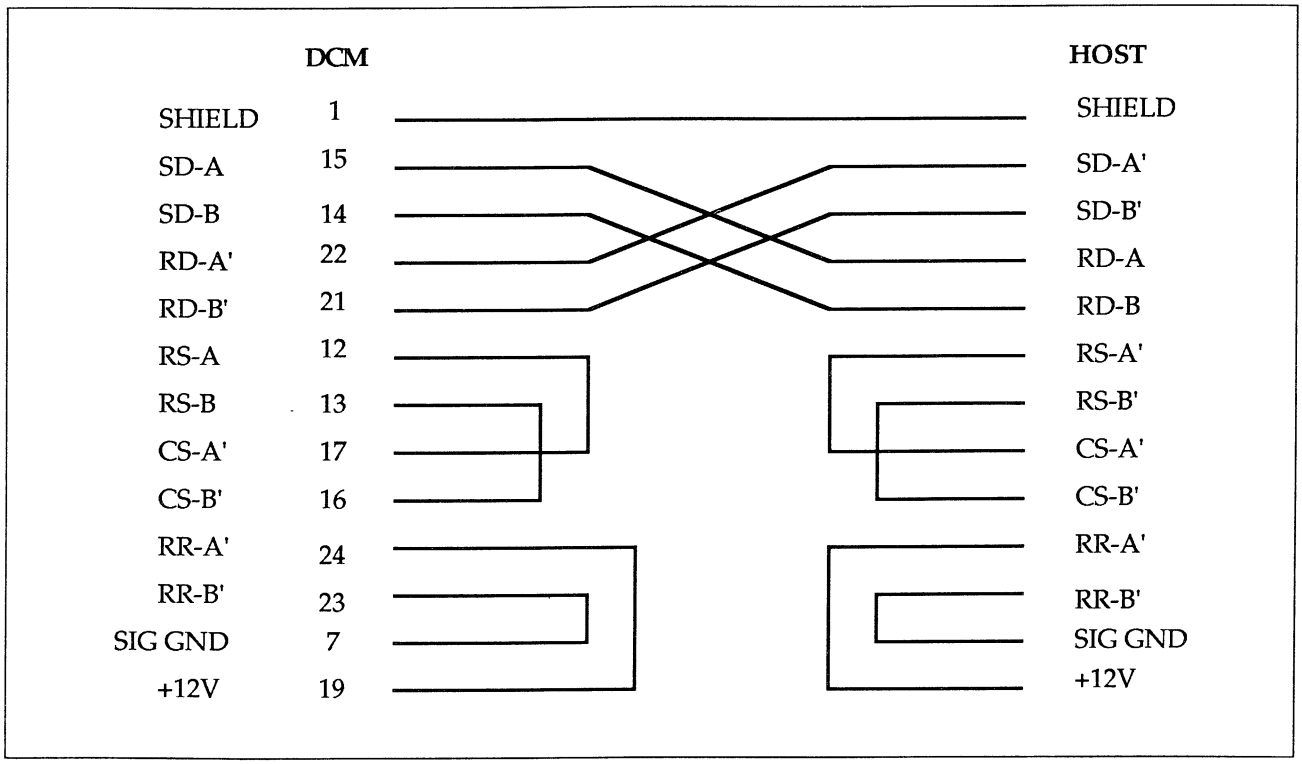
Figure 2-6 RS422/RS485 Connection to Minimum Function Modem



Continued on next page

DCM wiring diagrams,
continued

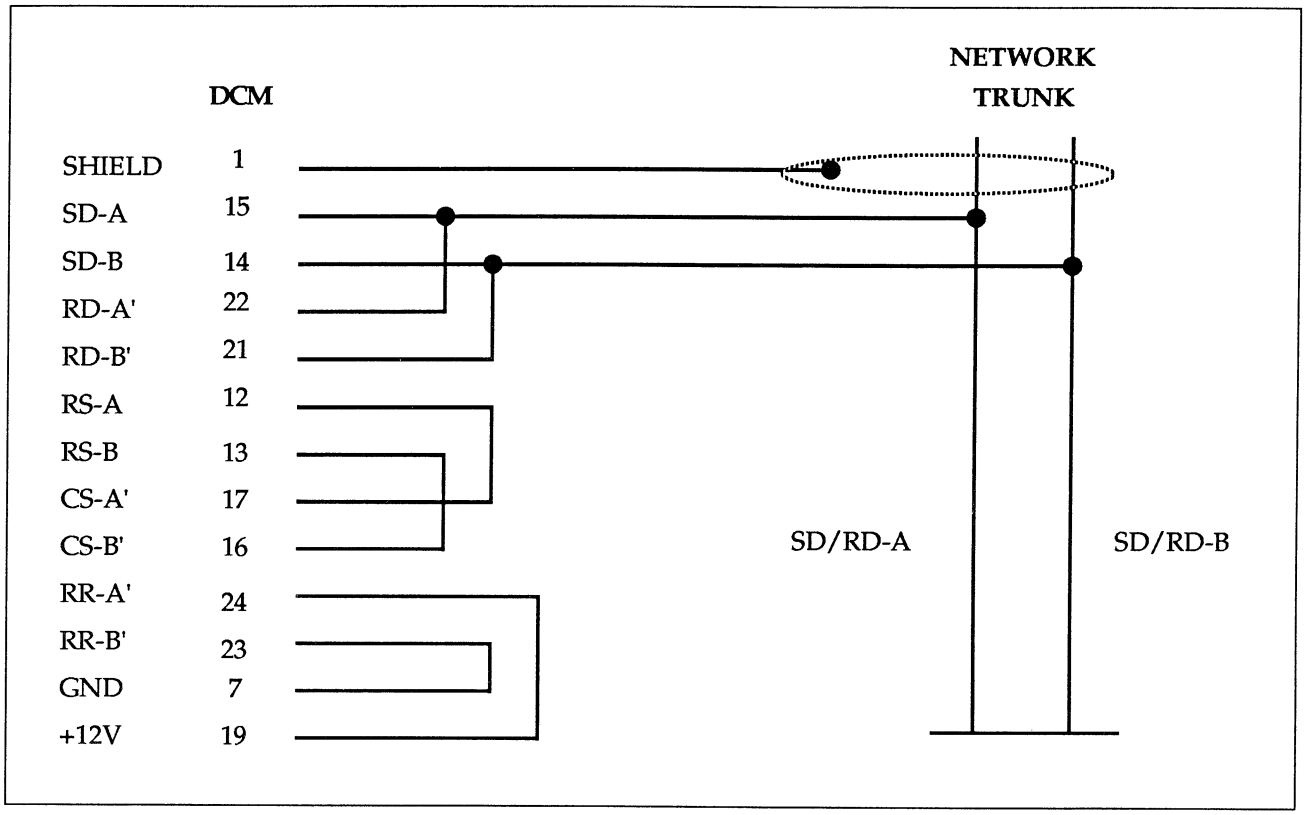
Figure 2-7 RS422/RS485 Connection to Host



Continued on next page

DCM wiring diagrams,
continued

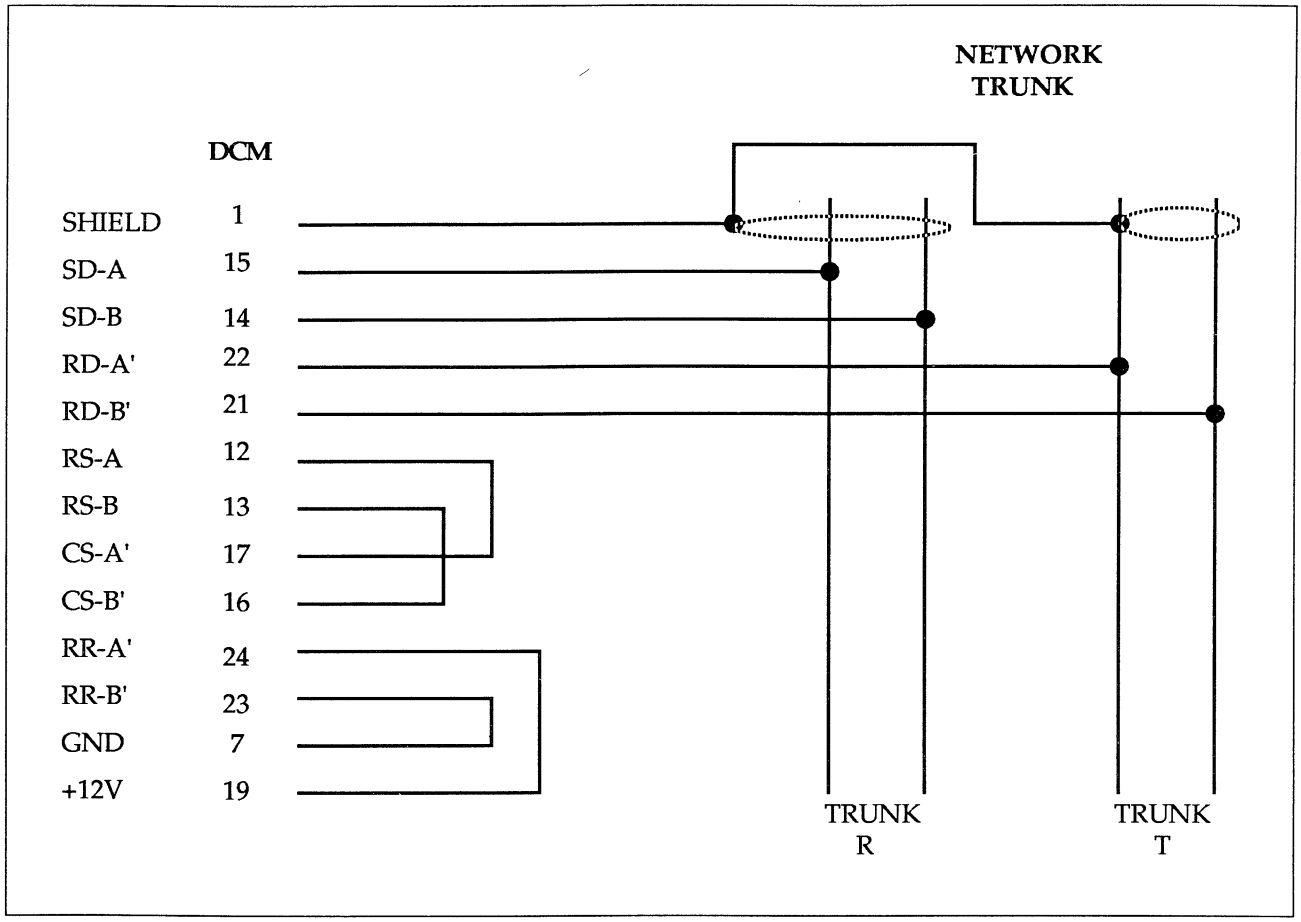
Figure 2-8 RS422/RS485 Single Twisted-Pair Network Connection



Continued on next page

DCM wiring diagrams,
continued

Figure 2-9 RS422/RS485 Two Twisted-Pair Network Connection



Section 3 – DCM Configuration

Overview

Section contents

Background

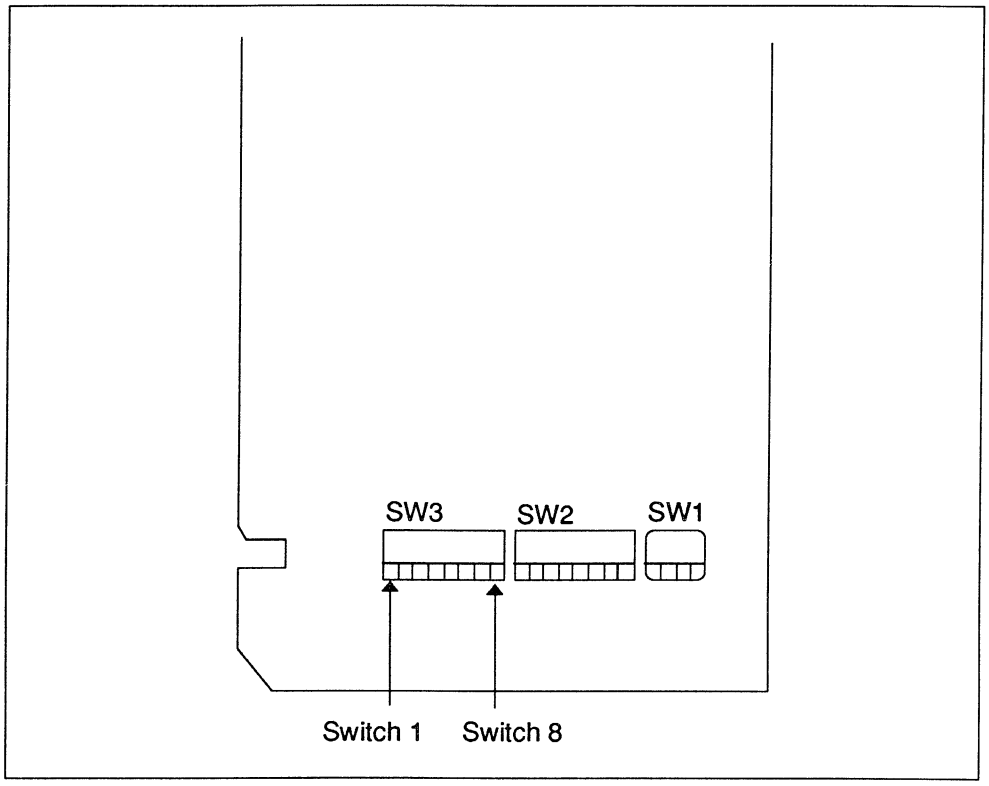
Certain parameters must be considered when the DCM is interfaced with a host computer. Selection of various options in each category allows you to configure the DCM to your particular application. Options are selected by means of DIP switch settings. Designate the DCM parameters by setting the DIP switches according to the procedures presented in this section for either the 620-0048 or 620-0052 DCM.

620-0048 DCM DIP Switch Settings

Setting 620-0048 DCM DIP switches

The single printed circuit board of the 620-0048 DCM is keyed to a receptive backplane. Three banks of DIP switches located on the lower edge of the module circuit board provide 20 DIP switches that control the DCM configuration. There are two 8-position and one 4-position DIP switch packs located on the module board as shown in Figure 3-1.

Figure 3-1 620-0048 DCM DIP Switches



Continued on next page

620-0048 DCM parameters

Refer to Table 3-1 for a list of the parameters and their controlling DIP switches to be considered when interfacing the 620-0048 DCM with a host computer.

Table 3-1 620-0048 DCM Parameters and DIP Switches

Parameter	DIP Switch
RS422 Receiver Termination	SW1 switch 1
Point-to-Point/Multipoint Select	SW1 switch 2
RS232 or RS422/RS485 Transmission	SW1 switch 3
One Stop Bit/Two Stop Bits	SW1 switch 4
Accept/Reject Instructions that Write to Program Memory	SW2 switch 1
Accept/Reject Instructions that Write to the Control Output Status Table	SW2 switch 2
Normal Operation/Flag Mode	SW2 switch 3
Nodal Address Select	SW2 switches 4 through 8
Baud Rate	SW3 switches 1 through 3
Parity Bit Enable/Disable	SW3 switch 4
Even/Odd Parity	SW3 switch 5
Spare	SW3 switch 6
Module Address Select	SW3 switches 7 and 8

Continued on next page

Setting 620-0048 DCM electrical parameters

620-0048 DCM electrical parameters include RS232 or RS422/RS485 interface, point-to-point or multidrop topology, and RS422 receiver termination (see Figure 3-2). Perform the procedure presented in Table 3-2 to set 620-0048 DCM electrical parameters.

Table 3-2 Setting 620-0048 DCM Electrical Parameters

Step	Action
1	Select physical interface. Set DCM for operation with an RS232 interface by positioning SW1 switch 3 in the CLOSED/ON state. Set DCM for operation with an RS422/RS485 interface by positioning SW1 switch 3 in the OPEN/OFF state.
2	Select topology with SW1 switch 2. Adjust for RS422 (RS485) multidrop operation by positioning SW1 switch 2 in the CLOSED/ON state. Enabling this function allows the DCM to operate in half-duplex mode. Enable point-to-point operation by placing SW1 switch 2 in the OPEN/OFF state.
3	If RS422 (RS485) multidrop operation is selected (SW1 switch 3 is OPEN/OFF), remove the 150-ohm resistor from RS422 RECEIVE DATA input from all DCMs except the one located at the physical end of the bus (see Figure 3-3). In that DCM, the 150-ohm resistor is enabled by positioning SW1 switch 1 in the CLOSED/ON state. In the other DCMs, the 150-ohm resistor is removed by positioning SW1 switch 1 in the OPEN/OFF state.

Continued on next page

SW1	Closed	Open
S1	150-ohm resistor added for point-to-point connections with RS422.	150-ohm resistor removed for multidrop connections with RS485.
S2	Configures RS422 transmitter for multidrop operation (RS485).	Configures RS422 transmitter for point-to-point operation, and DCM for full-duplex operation.

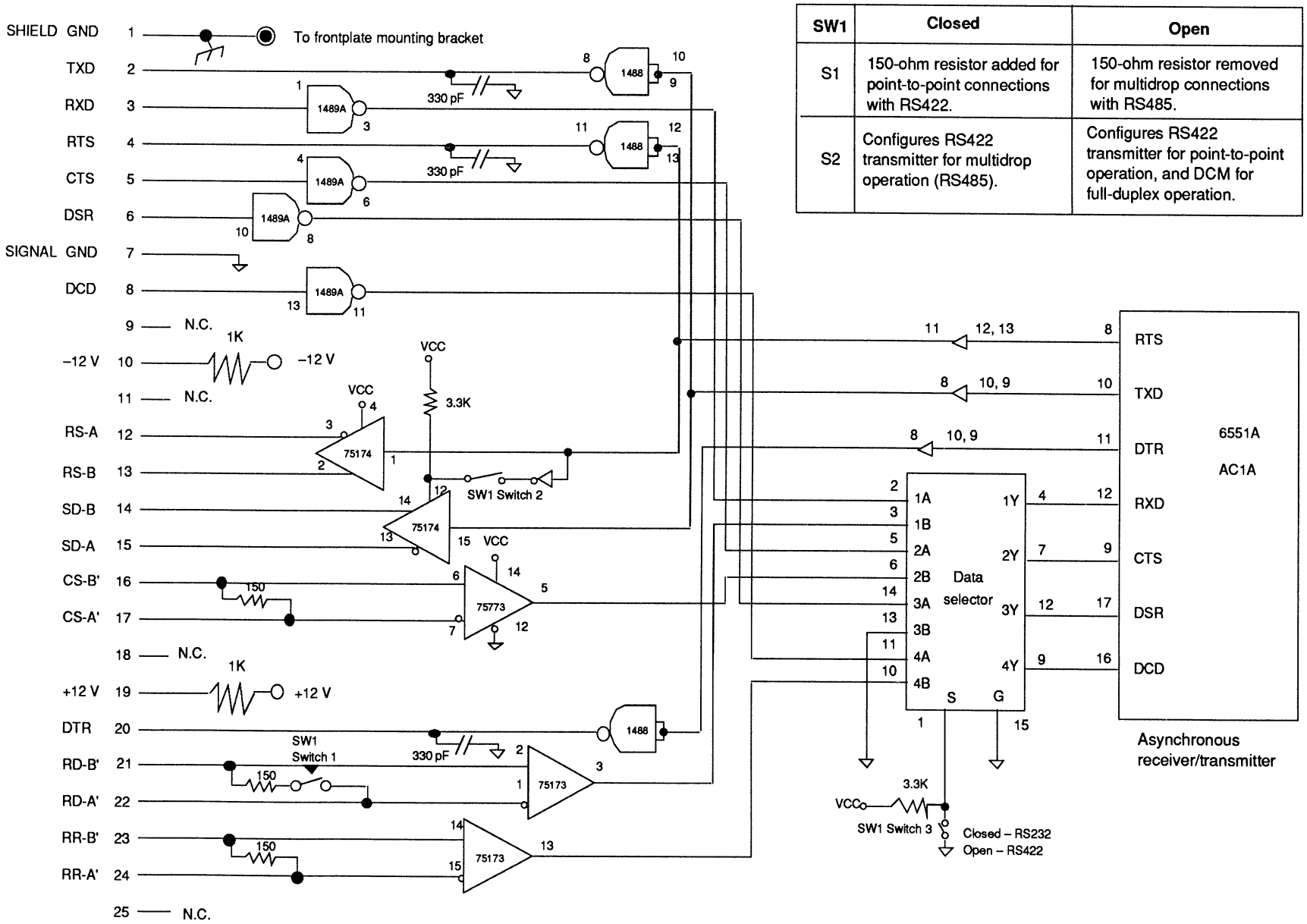
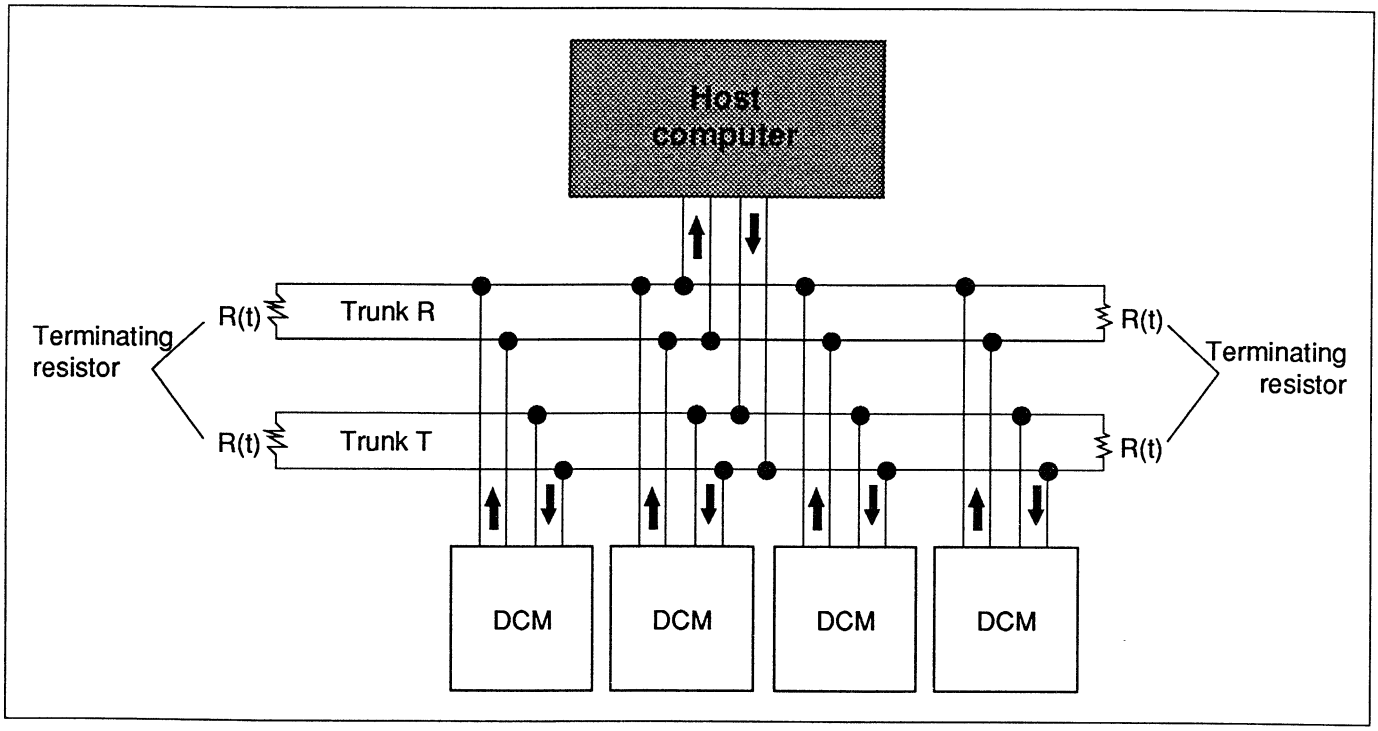


Figure 3-2 DCM Serial Port with Multidrop Control

Continued on next page

Setting 620-0048 DCM electrical parameters, continued

Figure 3-3 DCM Terminating Resistor Locations



Continued on next page

Setting 620-0048 DCM data link parameters

620-0048 DCM data link parameters include 620-0048 DCM nodal address, baud rate, and character format. Perform the procedure presented in Table 3-3 to set 620-0048 DCM data link parameters.

Table 3-3 Setting 620-0048 DCM Data Link Parameters

Step	Action
1	Select network nodal addresses from 0 through 31. Position SW2 switches 4, 5, 6, 7, and 8 to corresponding states (refer to Table 3-7). Each DCM must have a unique address. Zero is used as a broadcast nodal address.
2	Select DCM baud rate by positioning SW3 switches 1, 2, and 3 to states corresponding to selected baud rates (refer to Table 3-8). All DCMs on the network and the host must have the same baud rate.
3	Select parity with SW3 switch 4. Enable parity by positioning SW3 switch 4 to CLOSED/ON. Disable parity by positioning switch SW3 switch 4 to OPEN/OFF.
4	If parity is enabled (that is, SW3 switch 4 is CLOSED/ON), select the type of parity desired with SW3 switch 5. Select even parity by positioning SW3 switch 5 to OPEN/OFF. Select odd parity by positioning SW3 switch 5 to CLOSED/ON.
5	If parity is disabled (that is, SW3 switch 4 is OPEN/OFF), select the number of stop bits by positioning SW1 switch 4 to CLOSED/ON for one stop bit or OPEN/OFF for two stop bits.

Continued on next page

Setting 620-0048 DCM operational parameters

620-0048 DCM operational parameters include output write protect, normal mode or flag mode operation, and 620-0048 DCM card address. Perform the procedure presented in Table 3-4 to set 620-0048 DCM operational parameters.

Table 3-4 Setting 620-0048 DCM Operational Parameters

Step	Action
1	To accept instructions that write to program memory, set SW2 switch 1 to OPEN/OFF. To reject instructions that write to program memory, set SW2 switch 1 to CLOSED/OFF.
2	To accept instructions that write to the control output status table, to real outputs, or to the register table, set SW2 switch 2 to OPEN/OFF. To reject instructions that write to the control output status table, to real outputs, or to the register table, set SW2 switch 2 to CLOSED/ON.
3	To select normal mode operation, set SW2 switch 3 to CLOSED/ON. To select flag mode operation, set SW2 switch 3 to OPEN/OFF.
4	Select DCM card address by positioning SW3 switches 7 and 8 to states corresponding to selected addresses (refer to Table 3-10). Note that only certain addresses may be assigned to DCMs located in particular CPMs as follows:

CPM	Available Addresses
620-10/15	0
620-12/1633/36 †	0, 1, 2, or 3
620-20/30*	0 or 1
620-25/35*	0, 1, 2, or 3

† 620-1690/-1693 processor racks allow up to two DCMs and the 620-3691 processor rack allows up to four DCMs; each DCM must have a unique card address.

* If more than one DCM is installed in a 620-20/25 or 620-30/35 LCS, each must have a unique card address.

Continued on next page

620-0048 DCM SW1 DIP switch settings

Refer to Table 3-5 for 620-0048 DCM SW1 DIP switch settings.

Table 3-5 620-0048 DCM SW1 DIP Switch Settings

SW1 Switch	State	Function
1	CLOSED/ON*	Resistor added for point-to-point connections with RS422.
	OPEN/OFF	Resistor removed for multidrop connections with RS485.
2	CLOSED/ON	Configures RS422 transmitter for multipoint operation (RS485).
	OPEN/OFF*	Configures RS422 transmitter for point-to-point operation, and DCM for full-duplex operation.
3	CLOSED/ON	Selects RS232.
	OPEN/OFF	Selects RS422/RS485.
4	CLOSED/ON*	Selects one stop bit.
	OPEN/OFF	Selects two stop bits.

* Factory setting.

Continued on next page

620-0048 DCM SW2 DIP switch settings

Refer to Tables 3-6 and 3-7 for 620-0048 DCM SW2 DIP switch settings.

Table 3-6 620-0048 DCM SW2 DIP Switch Settings – Switches 1, 2, and 3

SW2 Switch	State	Function
1	CLOSED/ON*	DCM rejects instructions writing to program memory.
	OPEN/OFF	DCM accepts instructions writing to program memory.
2	CLOSED/ON	DCM rejects instructions writing to the control output status table, to real outputs, or to the register table.
	OPEN/OFF*	DCM accepts instructions writing to the control output status table, to real outputsts, or to the register table.
3	CLOSED/ON*	Selects normal mode operation.
	OPEN/OFF	Selects flag mode operation.

* Factory setting.

Continued on next page

620-0048 DCM SW2
DIP switch settings

Table 3-7 620-0048 DCM SW2 DIP Switch Settings – Switches 4, 5, 6, 7, and 8

Switch 4	Switch 5	Switch 6	Switch 7	Switch 8	ADDRESS
OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	0*
CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	1
OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	2
CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	3
OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	4
CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	5
OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	6
CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	7
OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	8
CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	9
OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	10
CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	11
OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	12
CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	13
OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	14
CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	15
OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	16
CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	17
OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	18
CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	19
OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	20
CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	21
OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	22
CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	23

* Factory setting.

Continued on next page

620-0048 DCM SW2 DIP switch settings, continued

Table 3-7 620-0048 DCM SW2 DIP Switch Settings – Switches 4, 5, 6, 7, and 8, Continued

Switch 4	Switch 5	Switch 6	Switch 7	Switch 8	ADDRESS
OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	**24**
CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	**25**
OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	**26**
CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	**27**
OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	**28**
CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	**29**
OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	**30**
CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	**31**

Continued on next page

620-0048 DCM SW3 DIP switch settings

Refer to Tables 3-8, 3-9, and 3-10 for 620-0048 DCM SW3 DIP switch settings.

Table 3-8 620-0048 DCM SW3 DIP Switch Settings – Switches 1, 2, and 3

Switch 1	Switch 2	Switch 3	Baud Rate
CLOSED/ON	CLOSED/ON	CLOSED/ON	110
OPEN/OFF	CLOSED/ON	CLOSED/ON	300
CLOSED/ON	OPEN/OFF	CLOSED/ON	600
OPEN/OFF	OPEN/OFF	CLOSED/ON	1200
CLOSED/ON	CLOSED/ON	OPEN/OFF	2400
OPEN/OFF	CLOSED/ON	OPEN/OFF	4800
CLOSED/ON	OPEN/OFF	OPEN/OFF	9600
OPEN/OFF	OPEN/OFF	OPEN/OFF	19.2K*

* Factory setting.

Table 3-9 620-0048 DCM SW3 DIP Switch Settings – Switches 4, 5, and 6

Switch 4	CLOSED/ON*	Parity bit enabled.
	OPEN/OFF	Parity bit disabled.
Switch 5	CLOSED/ON*	Odd parity.
	OPEN/OFF	Even parity.
Switch 6	CLOSED/ON*	Not used.
	OPEN/OFF	Not used

* Factory setting.

Table 3-10 620-0048 DCM SW3 DIP Switch Settings – Switches 7 and 8

Switch 7	Switch 8	Function
CLOSED/ON	CLOSED/ON	Card address 0 *
CLOSED/ON	OPEN/OFF	Card address 1
OPEN/OFF	CLOSED/ON	Card address 2
OPEN/OFF	OPEN/OFF	Card address 3

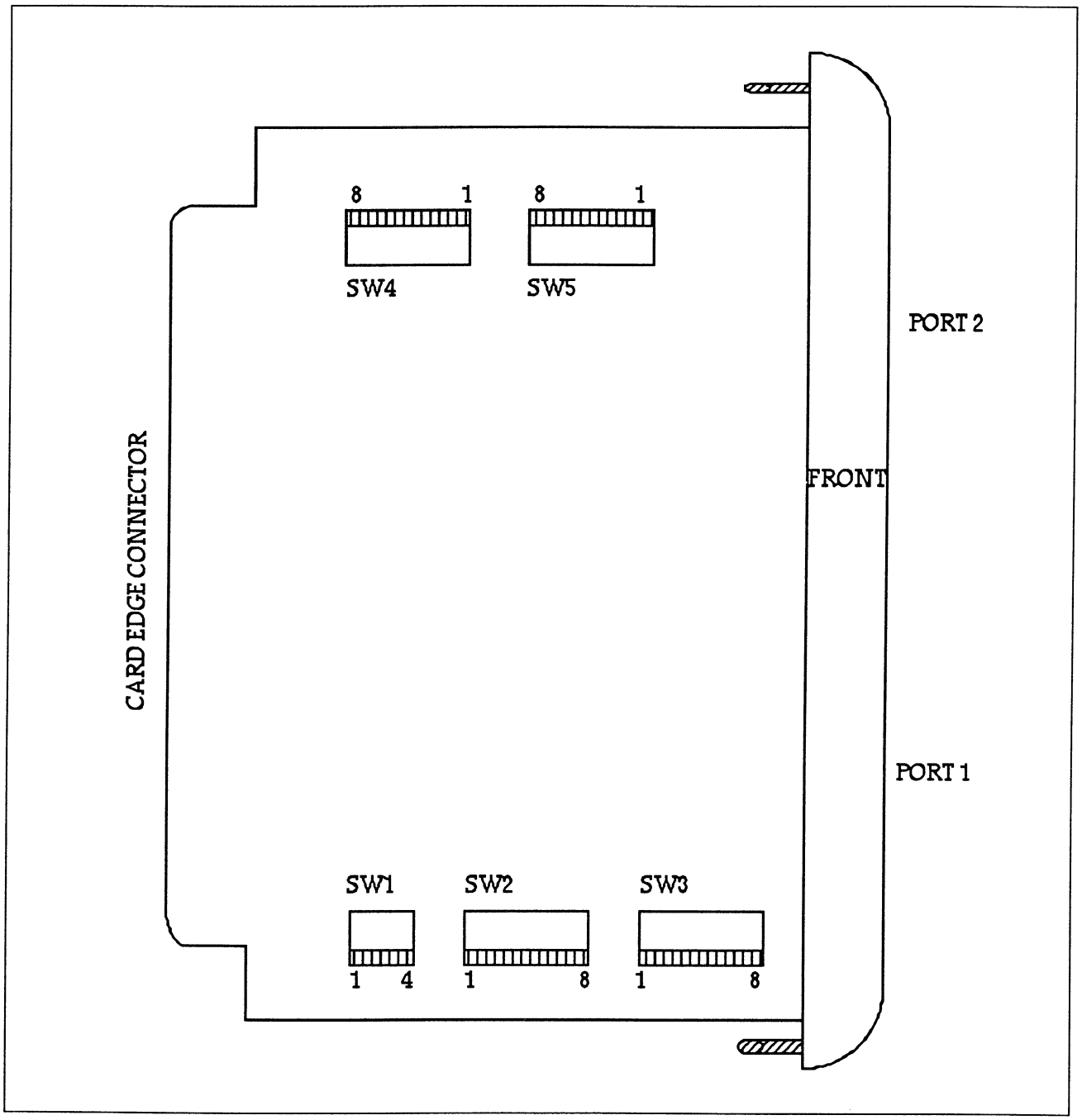
* Factory setting.

620-0052 DCM DIP Switch Settings

Setting 620-0052 DCM DIP switches

The single printed circuit board of the 620-0052 DCM is keyed to a receptive backplane. Five banks of DIP switches located on the module circuit board provide 36 DIP switches that control the DCM configuration. There are four 8-position and one 4-position DIP switch packs located on the module board as shown in Figure 3-4.

Figure 3-4 620-0052 DCM DIP Switches



Continued on next page

620-0052 DCM parameters

Refer to Table 3-11 for a list of the parameters and their controlling DIP switches to be considered when interfacing the 620-0052 DCM with a host computer.

Table 3-11 620-0052 DCM Parameters and DIP Switches

Parameter	DIP Switch
Module Address Select	SW1 switches 1 and 2
Normal Operation/Flag Mode – Port 1	SW1 switch 3
Normal Operation/Flag Mode – Port 2	SW1 switch 4
Nodal Address Select – Port 1	SW2 switches 1 through 5
RS232 or RS422/RS485 Transmission – Port 1	SW2 switch 6
Point-to-Point/Multidrop Select – Port 1	SW2 switch 7
RS422 Receiver Termination – Port 1	SW2 switch 8
Baud Rate – Port 1	SW3 switches 1 through 3
Parity Bit Enable/Disable – Port 1	SW3 switch 4
Even/Odd Parity – Port 1	SW3 switch 5
One Stop Bit/Two Stop Bits – Port 1	SW3 switch 6
Accept/Reject Instructions that Write to Program Memory – Port 1	SW3 switch 7
Accept/Reject Instructions that Write to the Control Output Status Table, Real Outputs, or Register Table – Port 1	SW3 switch 8
Nodal Address Select – Port 2	SW4 switches 1 through 5
RS232 or RS422/RS485 Transmission – Port 2	SW4 switch 6
Point-to-Point/Multidrop Select – Port 2	SW4 switch 7
RS422 Receiver Termination – Port 2	SW4 switch 8
Baud Rate – Port 2	SW5 switches 1 through 3
Parity Bit Enable/Disable – Port 2	SW5 switch 4
Even/Odd Parity – Port 2	SW5 switch 5
One Stop Bit/Two Stop Bits – Port 2	SW5 switch 6
Accept/Reject Instructions that Write to Program Memory – Port 2	SW5 switch 7
Accept/Reject Instructions that Write to the Control Output Status Table, Real Outputs, or Register Table – Port 2	SW5 switch 8

Continued on next page

Setting 620-0052 DCM electrical parameters

620-0052 DCM electrical parameters include RS232 or RS422/RS485 interface, point-to-point or multidrop topology, and RS422 receiver termination (see Figure 3-2). Perform the procedure presented in Table 3-12 to set 620-0052 DCM electrical parameters.

Table 3-12 Setting 620-0052 DCM Electrical Parameters

Step	Action
1	Select physical interface. Set DCM for operation with an RS232 interface by positioning SW2 switch 6 (for Port 1) or SW4 switch 6 (for Port 2) in the CLOSED/ON state. Set DCM for operation with an RS422/RS485 interface by positioning switch 6 in the OPEN/OFF state.
2	Select topology with SW2 switch 7 (for port 1) or SW4 switch 7 (for port 2). Adjust for RS422 (RS485) multidrop operation by positioning SW2 switch 7 (for Port 1) or SW4 switch 7 (for Port 2) in the CLOSED/ON state. Enabling this function allows the DCM to operate in half-duplex mode. Enable point-to-point operation by placing SW2 switch 7 (for Port 1) or SW4 switch 7 (for Port 2) in the OPEN/OFF state.
3	If RS422 (RS485) multidrop operation is selected (either SW2 switch 7 or SW4 switch 7 is CLOSED/OFF as specified in step 2), remove the 150-ohm resistor from RS422 RECEIVE DATA input from all DCMs except the one located at the physical end of the bus (see Figure 3-3). In that DCM, the 150-ohm resistor is enabled by positioning SW2 switch 8 (for Port 1) or SW4 switch 8 (for Port 2) in the CLOSED/ON state. In the other DCMs, the 150-ohm resistor is removed by positioning SW2 switch 8 (for Port 1) or SW4 switch 8 (for Port 2) in the OPEN/OFF state.

Continued on next page

Setting 620-0052 DCM data link parameters

620-0052 DCM data link parameters include 620-0052 DCM nodal address, baud rate, and character format. Perform the procedure presented in Table 3-13 to set 620-0052 DCM data link parameters.

Table 3-13 Setting 620-0052 DCM Data Link Parameters

Step	Action
1	Select network nodal addresses from 0 through 31. Position SW2 switches 1, 2, 3, 4, and 5 (for Port 1) or SW4 switches 1, 2, 3, 4, and 5 (for Port 2) to corresponding states (refer to Table 3-17). Each DCM must have a unique address. Zero is used as a broadcast nodal address.
2	Select DCM baud rate by positioning SW3 switches 1, 2, and 3 (for Port 1) or SW5 switches 1, 2, and 3 (for Port 2) to states corresponding to selected baud rates (refer to Table 3-19). All DCMs on the network and the host must have the same baud rate.
3	Select parity with SW3 switch 4 (for Port 1) or SW5 switch 4 (for Port 5). Enable parity by positioning switch 4 to CLOSED/ON. Disable parity by positioning switch 4 to OPEN/OFF.
4	If parity is enabled (that is, SW3 or SW5 switch 4 is CLOSED/ON as described in step 3), select the type of parity desired with SW3 switch 5 (for Port 1) or SW5 switch 5 (for Port 2). Select even parity by positioning switch 5 to OPEN/OFF. Select odd parity by positioning switch 5 to CLOSED/ON.
5	If parity is disabled (that is, SW3 switch 4 or SW5 switch 4 is OPEN/OFF as described in step 3), select the number of stop bits by positioning SW3 switch 6 (for Port 1) or SW5 switch 6 (for Port 2) to CLOSED/ON for one stop bit or OPEN/OFF for two stop bits.

Continued on next page

Setting 620-0052 DCM operational parameters

620-0052 DCM operational parameters include output write protect, normal mode or flag mode operation, and 620-0052 DCM card address. Perform the procedure presented in Table 3-14 to set 620-0052 DCM operational parameters.

Table 3-14 Setting 620-0052 DCM Operational Parameters

Step	Action
1	To accept instructions that write to program memory, set SW3 switch 7 (for Port 1) or SW5 switch 7 (for Port 2) to OPEN/OFF. To reject instructions that write to program memory, set SW3 switch 7 (for Port 1) or SW5 switch 7 (for Port 2) to CLOSED/OFF.
2	To accept instructions that write to the control output status table, to real outputs, or to the register table, set SW3 switch 8 (for Port 1) or SW5 switch 8 (for Port 2) to OPEN/OFF. To reject instructions that write to the control output status table, to real outputs, or to the register table, set SW3 switch 8 (for Port 1) or SW5 switch 8 (for Port 2) to CLOSED/ON.
3	To select normal mode operation, set SW1 switch 3 (for Port 1) or SW1 switch 4 (for Port 2) to CLOSED/ON. To select flag mode operation, set SW1 switch 3 (for Port 1) or SW1 switch 4 (for Port 2) to OPEN/OFF.
4	Select the DCM card address by positioning SW1 switches 1 and 2 to states corresponding to selected addresses (refer to Table 3-15). Note that only certain addresses may be assigned to DCMs located in particular CPMs as follows:

CPM	Available Addresses
620-10/15	0
620-12/1633/36 †	0, 1, 2, or 3
620-20/30*	0 or 1
620-25/35*	0, 1, 2, or 3

† 620-1690/-1693 processor racks allow up to two DCMs and the 620-3691 processor rack allows up to four DCMs; each DCM must have a unique card address.

* If more than one DCM is installed in a 620-20/25 or 620-30/35 LCS, each must have a unique card address.

Continued on next page

620-0052 DCM DIP Switch Settings, Continued

620-0052 DCM SW1 DIP switch settings

Refer to Tables 3-15 and 3-16 for 620-0052 DCM SW1 DIP switch settings.

Table 3-15 620-0052 DCM SW1 DIP Switch Settings – Switches 1 and 2

Switch 1	Switch 2	Function
CLOSED/ON	CLOSED/ON	Card address 0 *
OPEN/OFF	CLOSED/ON	Card address 1
CLOSED/ON	OPEN/OFF	Card address 2
OPEN/OFF	OPEN/OFF	Card address 3

* Factory setting.

Table 3-16 620-0052 DCM SW1 DIP Switch Settings – Switches 3 and 4

SW1 Switch	State	Function
3	CLOSED/ON*	Port 1 – Normal mode of operation.
	OPEN/OFF	Port 1 – Flag mode of operation.
4	CLOSED/ON	Port 2 – Normal mode of operation.
	OPEN/OFF*	Port 2 – Flag mode of operation.

* Factory setting.

Continued on next page

620-0052 DCM SW2 and SW4 DIP switch settings

Refer to Tables 3-17 and 3-18 for 620-0052 DCM SW2 and SW4 DIP switch settings.

Table 3-17 620-0052 DCM SW2 (for Port 1) and SW4 (for Port 2) DIP Switch Settings – Switches 1, 2, 3, 4, and 5

Switch 1	Switch 2	Switch 3	Switch 4	Switch 5	ADDRESS
OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	0*
CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	1
OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	2
CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	3
OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	4
CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	5
OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	6
CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	7
OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	8
CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	9
OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	10
CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	11
OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	12
CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	13
OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	14
CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	15
OPEN/OFF	OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	16
CLOSED/ON	OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	17
OPEN/OFF	CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	18
CLOSED/ON	CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	19
OPEN/OFF	OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	20
CLOSED/ON	OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	21
OPEN/OFF	CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	22
CLOSED/ON	CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	23

* Factory setting.

Continued on next page

620-0052 DCM SW2 and SW4 DIP switch settings, continued

Table 3-17 620-0052 DCM SW2 (for Port 1) and SW4 (for Port 2) DIP Switch Settings – Switches 1, 2, 3, 4, and 5, Continued

Switch 1	Switch 2	Switch 3	Switch 4	Switch 5	ADDRESS
OPEN/OFF	OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	**24**
CLOSED/ON	OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	**25**
OPEN/OFF	CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	**26**
CLOSED/ON	CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	**27**
OPEN/OFF	OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	**28**
CLOSED/ON	OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	**29**
OPEN/OFF	CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	**30**
CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	CLOSED/ON	**31**

Table 3-18 620-0052 DCM SW2 (for Port 1) and SW4 (for Port 2) DIP Switch Settings – Switches 6, 7, and 8

Switch 6	CLOSED/ON	Selects RS232.
	OPEN/OFF*	Selects RS422/RS485.
Switch 7	CLOSED/ON	Configures RS422 transmitter for multidrop operation (RS485).
	OPEN/OFF*	Configures RS422 transmitter for point-to-point operation, and DCM for full-duplex operation.
Switch 8	CLOSED/ON*	Resistor added for point-to-point connections with RS422 interface.
	OPEN/OFF	Resistor removed for multidrop connections with RS422 interface.

* Factory setting.

Continued on next page

620-0052 DCM SW3 and SW5 DIP switch settings

Refer to Tables 3-19 and 3-20 for 620-0052 DCM SW3 and SW5 DIP switch settings.

Table 3-19 620-0052 DCM SW3 (for Port 1) and SW5 (for Port 2) DIP Switch Settings – Switches 1, 2, and 3

Switch 1	Switch 2	Switch 3	Baud Rate
CLOSED/ON	CLOSED/ON	CLOSED/ON	110
OPEN/OFF	CLOSED/ON	CLOSED/ON	300
CLOSED/ON	OPEN/OFF	CLOSED/ON	600
OPEN/OFF	OPEN/OFF	CLOSED/ON	1200
CLOSED/ON	CLOSED/ON	OPEN/OFF	2400
OPEN/OFF	CLOSED/ON	OPEN/OFF	4800
CLOSED/ON	OPEN/OFF	OPEN/OFF	9600
OPEN/OFF	OPEN/OFF	OPEN/OFF	19.2K*

* Factory setting.

Table 3-20 620-0052 DCM SW3 (for Port 1) and SW5 (for Port 2) DIP Switch Settings – Switches 4, 5, 6, 7, and 8

Switch 4	CLOSED/ON*	Parity bit enabled.
	OPEN/OFF	Parity bit disabled.
Switch 5	CLOSED/ON*	Odd parity.
	OPEN/OFF	Even parity.
Switch 6	CLOSED/ON*	One stop bit.
	OPEN/OFF	Two stop bits.
Switch 7	CLOSED/ON*	Rejects instructions writing to program memory.
	OPEN/OFF	Accepts instructions writing to program memory.
Switch 8	CLOSED/ON	Rejects instructions writing to the control output status table, real outputs, or register table.
	OPEN/OFF*	Accepts instructions writing to the control output status table, real outputs, or register table.

* Factory setting.

Section 4 – DCM Theory of Operation

Overview

Section contents

Option module to processor procedures

The Control Network Module (CNM), Data Collection Module (DCM), and Communications Interface Module (CIM) are 620 LCS option modules used for network communications. These modules read and write processor memory for control and data collection purposes. The modules perform the read/write functions transparently, without user memory programming.

The CNM, DCM, and CIM are intelligent modules controlled by microprocessors. A window of time occurs in the processor control cycle for each module to exchange data with the processor. The placement of windows and the methods of data exchange vary among the CNM, DCM, and CIM. The following descriptions summarize how the CNM, DCM, and CIM are "sysgened" within the processor, where the data exchange windows fall in the processor control loop, and how the data exchanges are accomplished.

Continued on next page

Option module system generation (sysgen)

The sysgen process is an identification/recording sequence that the processor performs as the last step in the self-test routine performed during power-up or PROGRAM-to-RUN mode changes. The processor attempts to identify any CNM, DCM, or CIM option modules residing in the processor rack.

The identification process consists of polling each card address of each module type until all have been polled or until the processor rack option module limit has been reached. The status and module addresses of the option module that respond are recorded; the modules then become eligible for window time during normal processor operation. The DCMs and CIMs are sysgened before the CNMs.

Refer to Table 4-1 for a summary of the sysgen process:

Table 4-1 Summary of the Sysgen Process

Step	Action
1	DCMs and CIMs are polled before CNMs.
2	The polling stops after the rack limit or module card address limits are reached.
3	Modules are polled from low to high address.
4	A valid reaction to a poll is required before a module is recorded and given eligibility for exchange windows.

Continued on next page

CIM/DCM sysgen

The 620 LCS provides a window for the DCM to update its status for each module address of 0 through 3 depending on the processor. This is a short window (1 ms or less) and is intended only for diagnostic status updates. Limited backplane diagnostics may be carried out by the DCM during this interval however.

CNM sysgen

The 620 LCS initiates a diagnostic/identify exchange with each CNM for each card address of 0 through 7. Any resident CNM that properly responds to this exchange is listed in the System Status Table and is eligible for exchange windows during contact input of the processor's RUN mode operation.

CIM/DCM exchange windows

Any DCM listed as present and functional by the processor is given a window at Memory Word Zero (MWZ) in which to carry out any data exchange requirements. Each functional module is checked for the assertion of "bus request" and, if the request is present, the window is granted. The window size can be as long as 40 ms (90 ms in the 620-11/14/1631 LCSs). After this time, the DCM is warned of a window timeout.

If the DCM fails to remove the bus request in 1 ms, the module is disconnected and reduced to a present/nonfunctional status. The DCM receives sysgen windows in place of data exchange windows while the DCM is listed as present/nonfunctional. The data collection function can increase the window up to 10 ms, not exceeding a total window size of 40 ms (90 ms in the 620-11/14/1631 LCSs).

The DCM windows are provided at MWZ just before the processor checks for module change inputs. The windows are given sequentially, from the lowest module address to the highest. The size of the window is generally much shorter than 40 ms (90 ms in the 620-11/14/1631 LCSs) and depends on the exchange taking place (for example, a read of 10 I/O points by a DCM takes several hundred microseconds).

Continued on next page

CNM exchange windows

Any CNM listed as present and functional by the 620 LCS is eligible for a data exchange sequence. This sequence occurs during any contact input that includes the first word in user memory. As a result, the CNMs receive windows only when the processor is scanning user memory (RUN mode).

If the CNM fails to properly participate in the data exchange results, its status changes to present/nonfunctional. When a CNM is listed as present/nonfunctional, it receives sysgen sequence commands instead of table exchange commands until its status is changed to present/functional or to not present.

The CNM windows occur in order from lowest to highest module address. The length of the CNM window varies among the 620-06/10/15 LCSs, the 620-11/14/1631 LCSs, the 620-12/1633/36 LCSs, and the 620-20/25/30/35 LCSs. Reading and writing relay or register data tables also affects the window length. Generally, the window is 1.6 to 3.2 ms per module.

CIM/DCM exchange procedures

The DCM data exchange procedures are more independent than the CNM procedures. The DCM has control of the system during its data exchange window, commanding the processor to carry out the data transfers. The DCM is responsible for writing its own status into the processor status table. From input commands in its external serial interface, it determines the type of data exchanges to be made with the processor. The DCM can be considered an independent processor that receives a time slot during which it controls the processor and manipulates various processor memories. The processor allows the DCM control only for the time period determined by this window.

The processor "disconnects" the DCM after that time period has passed if the DCM does not relinquish control.

CNM exchange procedures

The CNM operates as a slave to the 620 LCS. The data exchanges between the CNM and the LCS are initiated by opcodes from the processor module and are carried out in a predefined sequence of transfers. The CNM can be compared to a memory module that the processor accesses to read and write control data.

DCM Operation

Background

Both the 620-0048 and 620-0052 DCM each provide a specialized communications interface between computers and the 620 LCS. Each module accepts commands via its serial port, carries out the data exchange requested, and returns a response to the host computer.

DCM self-test

The DCM performs a self-test sequence upon application of line power to the 620 LCS in which the DCM is installed. Events of the sequence are reflected in the status of the PASS, ACTIVE, and FAULT LED indicators on the front panel of the module. Refer to Table 4-2 for an outline of the sequence.

Table 4-2 DCM Self-Test Sequence

Stage	DCM Status	PASS LED	ACTIVE LED	FAULT LED
1	Startup/initialization	OFF	ON	ON
2	DCM self-test	OFF	OFF	ON
3	DCM ready and waiting for processor system generation exchange	ON	OFF – inactive ON – active	ON
4	DCM ready and processor system generation successfully completed	ON	OFF – inactive ON – active	OFF
5	DCM ready and processor system generation faulty	ON	OFF – inactive ON – active	ON

Continued on next page

Self-test — first stage

The first stage of the self-test is initialization, during which the PASS LED is in the OFF state and the ACTIVE and FAULT LEDs are both in the ON state. The ACTIVE LED is energized to allow a visual check of system operation.

Self-test — second stage

The second stage is the DCM self-test. During this test the PASS and ACTIVE LEDs are both in the OFF state and the FAULT LED is in the ON state.

Self-test — third stage

The third stage is initiated after the DCM successfully completes the self-test. During this stage, the DCM waits for completion of the 620 LCS system generation. The PASS and FAULT LEDs are both in the ON state and the ACTIVE LED is in either the OFF or ON state depending on whether serial power is active. At this stage, the function of the ACTIVE LED changes from indicating DCM status to indicating serial port activity.

Self-test — fourth stage

The fourth stage occurs only if the processor successfully completes system generation. The PASS LED is in the ON state, the ACTIVE LED is in either the OFF or ON state depending on whether the serial port is active, and the FAULT LED is in the OFF state. From this stage the DCM enters the flow diagram (see Figure 4-1) at DCM EXECUTIVE.

Self-test — fifth stage

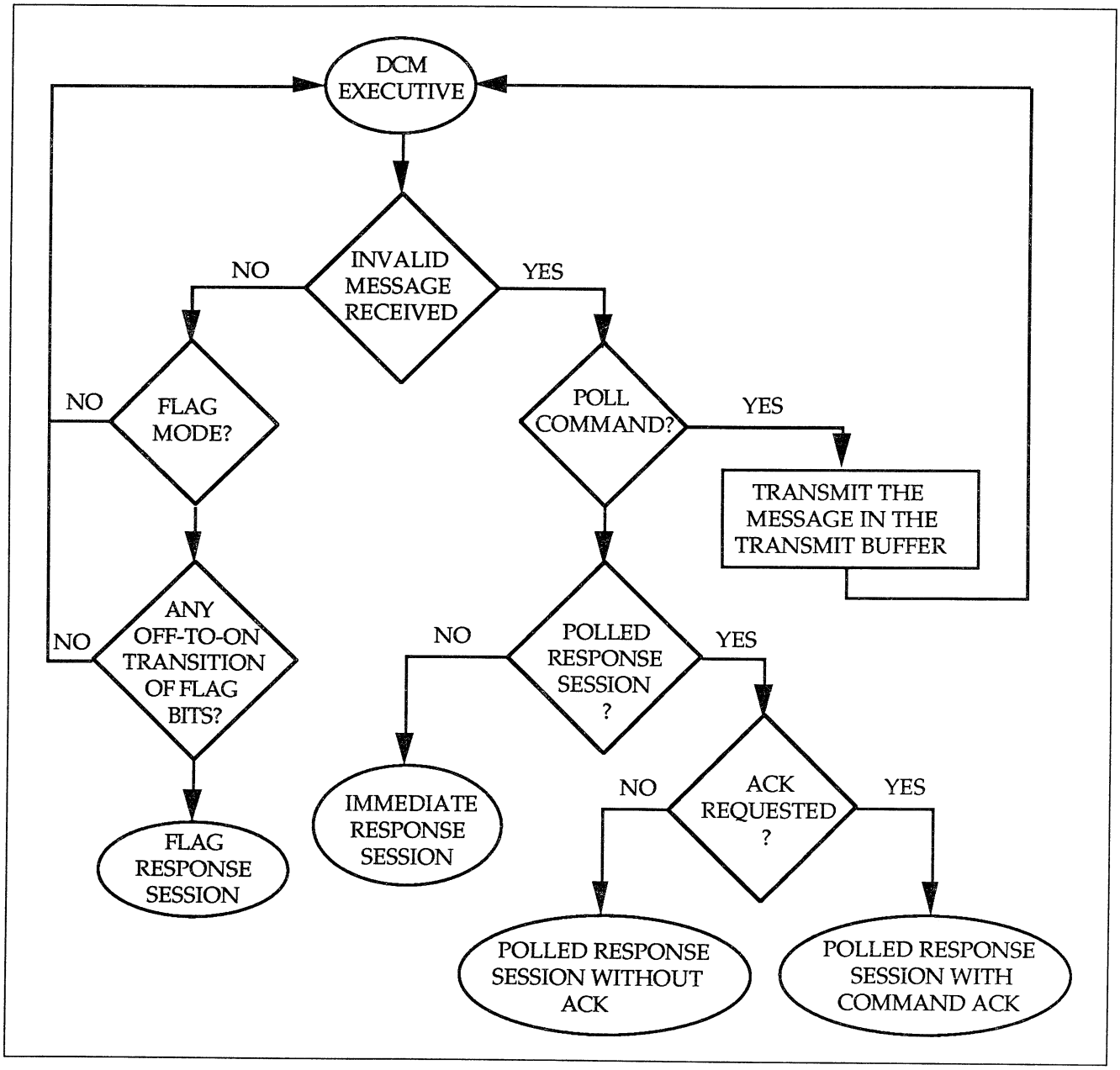
The fifth stage occurs only if the processor system generation fails to complete. The PASS and FAULT LEDs are both in the ON state, and the ACTIVE LED is in either the OFF or ON state depending on whether the serial port is active. The DCM attempts to return to the fourth stage from this stage, and continues to do so until the fourth stage is successfully completed.

Continued on next page

DCM response mode flow diagram

Refer to Figure 4-1 for the point where the DCM enters the flow diagram at DCM EXECUTIVE from stage four of the DCM self test.

Figure 4-1 DCM Response Mode Flow Diagram



Continued on next page

DCM response time

When the DCM requests it, the 620 LCS gives the DCM a time slot at the end of the program scan. The DCM is synchronized to processor scan and partially dependent on the processor scan for its response time to receive commands. During the time slot given, the DCM has access to the processor's I/O status, register contents, system registers, and program memory.

Read/write instructions

I/O status tables, registers, and system registers can be read while the 620 LCS is in the PROGRAM, RUN/PROGRAM, RUN, or DISABLE mode. Tables and registers can be written in any mode. If the processor is in the DISABLE or PROGRAM mode, the write instruction writes only to the status table locations. The real I/O is not updated. If the processor is in RUN or RUN/PROGRAM, the write instruction writes to the status table, and the processor updates the real I/O. (Refer to *Data Collection Mode* for more information on the DCM I/O status tables.)

Uploading/downloading program memory

Program memory can be uploaded or downloaded while the 620 LCS is in the PROGRAM, RUN/PROGRAM, RUN, or DISABLE mode. Only one peripheral device can be downloading program memory at one time.

DCM Data Link Control

Background

The 620-0048 and 620-0052 DCMs each use an Asynchronous Byte Count (ABC) protocol defined by Honeywell which is designed for use in localized point-to-point and multidrop applications. The ABC protocol accommodates the use of modems where RTS is the only active modem control line involved. Special data encoding (for example, ASCII) or control character insertion and deletion is unnecessary because of data transparency. This simplifies the process of developing communications.

ATTENTION

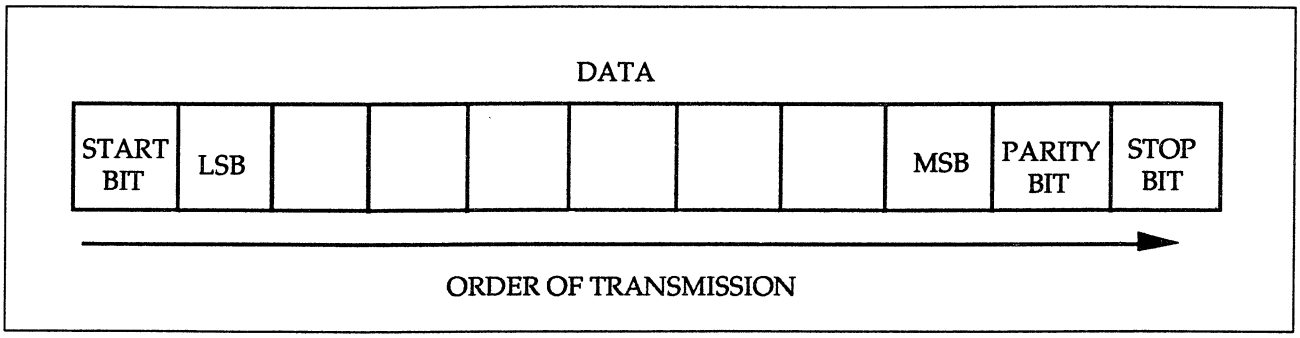
- The ABC protocol procedures are written for general data link control, however, they involve characteristics specific to the DCM.
- Refer to Section 5 for a complete listing of the DCM instruction set.

Continued on next page

Message structure

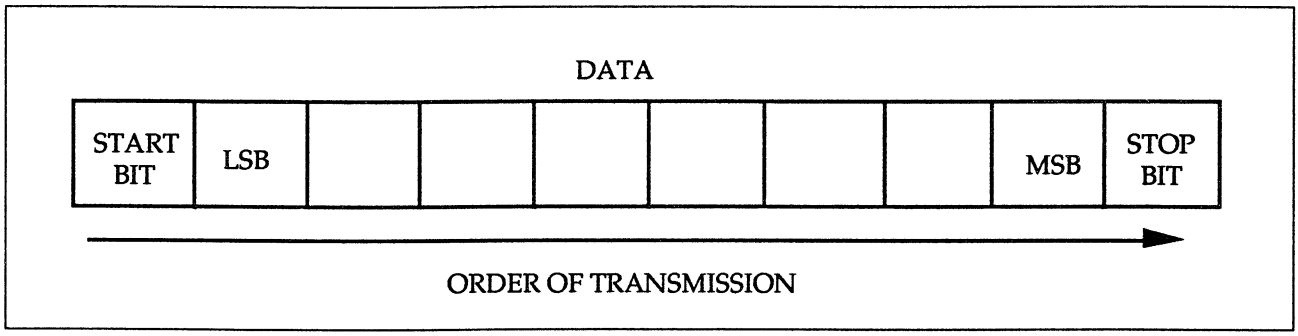
Standard configuration character format contains 11 bits (start, 8 data, parity, and stop) and has odd parity (see Figure 4-2).

Figure 4-2 ABC Protocol Character Format



Optional configuration character format contains 10 bits (start, 8 data, stop) (see Figure 4-3).

Figure 4-3 ABC Protocol Optional Character Format

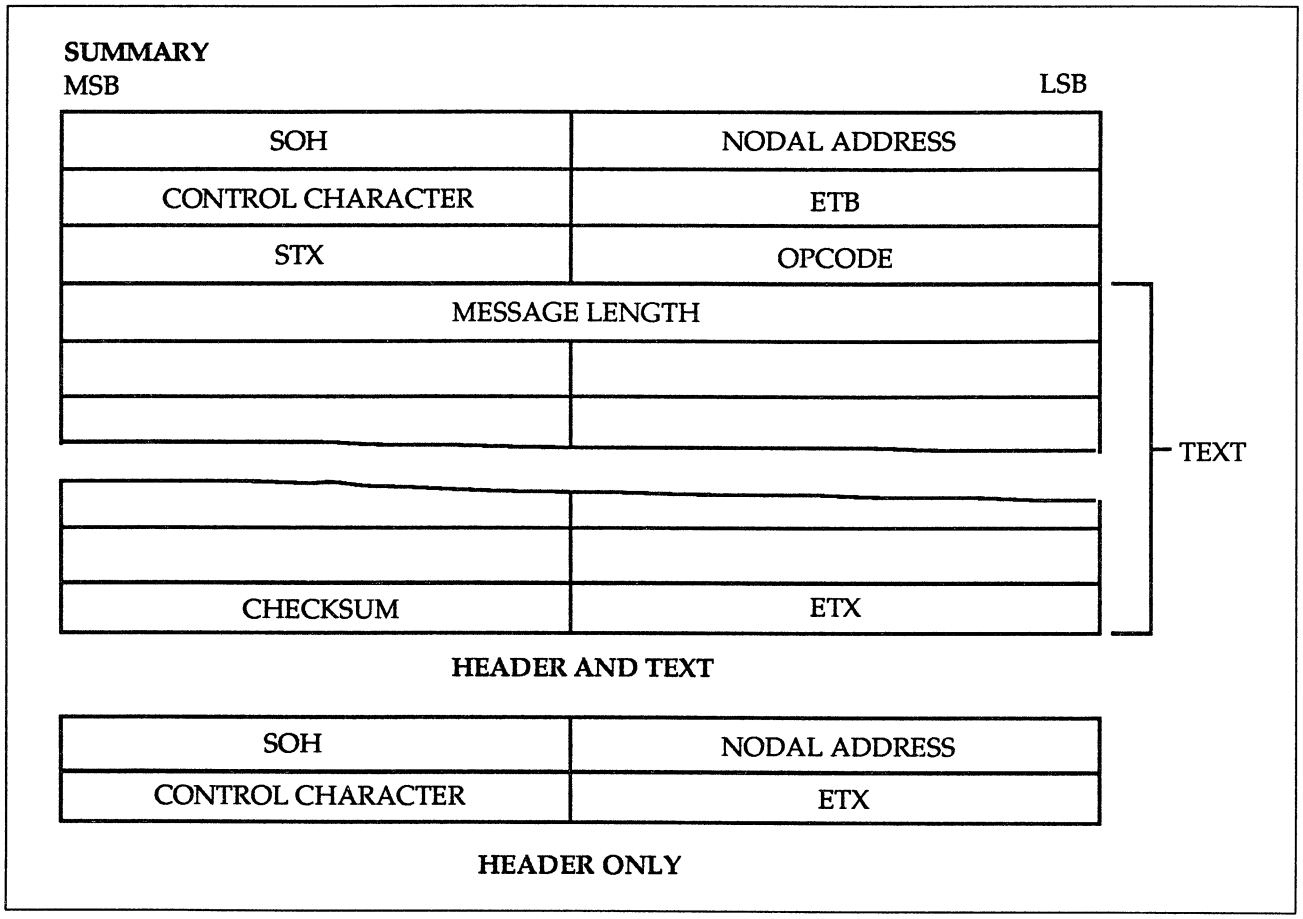


Continued on next page

Message format

Refer to Figure 4-4 for header and text message format (detailed explanations of each character function are presented in Table 4-3).

Figure 4-4 Header and Text Message Format



Continued on next page

Message format, continued

Table 4-3 Character Functions Used in Header and Text Message Format

Character Function	Description
SOH	(1) Start of header; 8 bits.
Nodal Address	An 8-bit binary number that identifies the secondary station involved in the message exchange. Addresses available for DCM applications range from 0 to 31. No two devices may have the same nodal address if the secondaries are to respond to received commands. Nodal address 255 is reserved for broadcast applications.
Control Character	An 8-bit character that identifies the message type.
ETB	(23) End of transmission block; 8 bits.
STX	(2) Start of text; 8 bits.
Opcode	This is the first character of the text and is defined by the application; it consists of 8 bits and identifies the type of operation that the receiving device is to perform. This character is 0 in response messages to the host device.
Message Length	16-bit binary number that specifies the number of characters in the message text; the upper limit of this value depends on the buffer size of the devices involved.
Text	Consists of 16-bit words that contain opcode modifiers, and/or data. Data less than 16 bits is justified to the least significant byte of the word.
Checksum	8-bit byte that represents the binary addition, with carry-between bits of each character between and including the nodal address and the last text character (refer to *DCM Program Memory Checksum* in this section).
ETX	(3) End of text.

Continued on next page

Message types

The ABC protocol includes two types of messages — supervisory and informational — which are identified by a control character. Refer to Table 4-4 for a list of host message types and identifying characters, and refer to Table 4-5 for a list of secondary message types and identifying characters.

Table 4-4 Host Message Types Summary

Control Character	Message	Description
1	Command Information/ Immediate Response	The host initiates this information message, which requests the DCM to execute the command and to respond with the results.
2	Command Information/ Polled Response Acknowledgement Requested	The host initiates this information message. The message requests an immediate acknowledgement of the command reception. At a later time, a poll command requests the results of the command execution.
4	Poll	This command message from the host requests transmission or retransmission of the contents of the secondary station's transmit buffer. This command requires only the header portion to be transmitted.
130	Command Information/ Polled Response/ No Acknowledge	The host initiates this information message. The message request is not acknowledged when the command is received. At a later time, a poll command requests the results of the command execution. Nodal address 255 is used as a global nodal address to transmit to all devices on the network. It can be used only with control character 130.

Continued on next page

Message types, continued

Table 4-5 Secondary Message Types Summary

Control Character	Message	Description
129	Response Information	This information message is in response to a host command or poll. This message is stored in the secondary station's buffer until it is overwritten during the execution of a subsequent command. As a result, the DCM may be repeatedly polled for retransmission of this message.
130	Acknowledge	This response from the secondary station indicates a valid command was received. The acknowledge is sent only upon request by the host (command information/polled response message). This response requires only the header portion to be transmitted.
132	Flag	A command by the secondary station that signifies a change in predetermined status bits within the secondary station. The text field contains the status information. This command requires both header and text to be transmitted.

Continued on next page

Order of transmission

The most significant byte of the 16-bit word precedes the least significant byte. The words are transmitted in order from SOH/nodal address to checksum/ETX.

DCM receiver limitations

The DCM receive buffer is 920 bytes. The DCM compares the message length character of any incoming instruction with the available buffer space. Any instruction that exceeds the buffer space is rejected.

The DCM receiver is capable of receiving an instruction plus one additional instruction if buffer limits are not exceeded. The second instruction places the following restrictions on the DCM:

- The DCM receiver is disabled when an instruction is being processed.
- If the first instruction requires a response to be transmitted, the second message received is not processed until the transmission of the first instruction response is completed. In such applications, the first instruction's response will be overwritten by the second instruction's response, unless the second instruction is a poll command.

The receiver buffer does not hold the complete received instruction. The DCM receiver firmware removes the following characters:

- Start of header (SOH),
- End of transmission block (ETB),
- Start of text (STX), and
- End of text (ETX).

DCM transmitter limitations

The transmit buffer on the 620-0048 holds 2063 bytes. The buffer on each port of the 620-0052 holds 2063 bytes. The limitations placed on received instructions prevent this buffer from overloading because of any response created by the DCM.

The DCM does not act on a received instruction until the completion of any response in progress; therefore, the transmit buffer does not become stacked with responses.

Continued on next page

Message reception timeout delays

The intercharacter delay facilitates effective fault and abort detection. A delay of ten character times or more between the reception of any two adjacent characters within a message results in an abort of the receive sequence.

To facilitate the use of software timers in the receiving stations, the ten-character timeout applies only to a receiver that is concentrating on the reception of the message. If a given receiver is distracted for X seconds to service an earlier message or another type of input, the abort timeout extends by X seconds. This gives the receiver the option to ignore the software timer while servicing other requests.

DCM Exchange Procedures

Background

The ABC protocol defines four exchange procedures which are available to the host computer and secondary devices:

- Immediate response
- Polled response without acknowledge
- Polled response with acknowledge
- Flag response

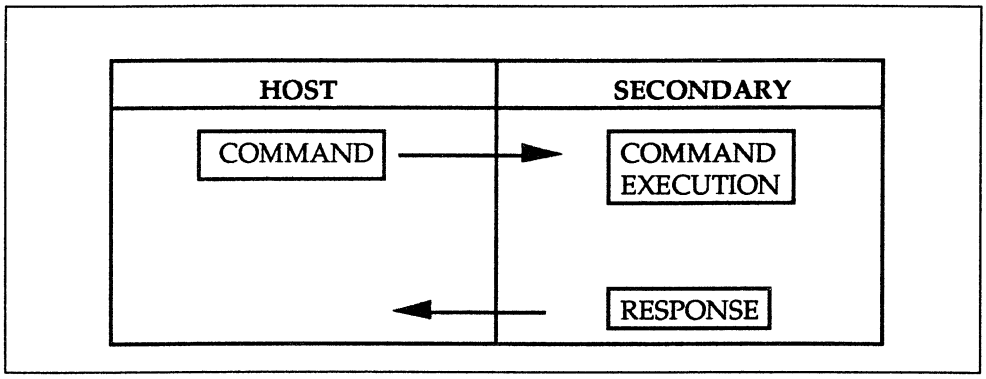
The DCM enters these response modes according to the flow diagram in Figure 4-1.

Continued on next page

Immediate response session

With the immediate response procedure, the host issues a command message and the secondary executes the command; then the secondary returns a result response (see Figure 4-5). Fail-safe timeout delays within the host depend on the command issued. The host relinquishes line control while awaiting the response.

Figure 4-5 Immediate Response Diagram

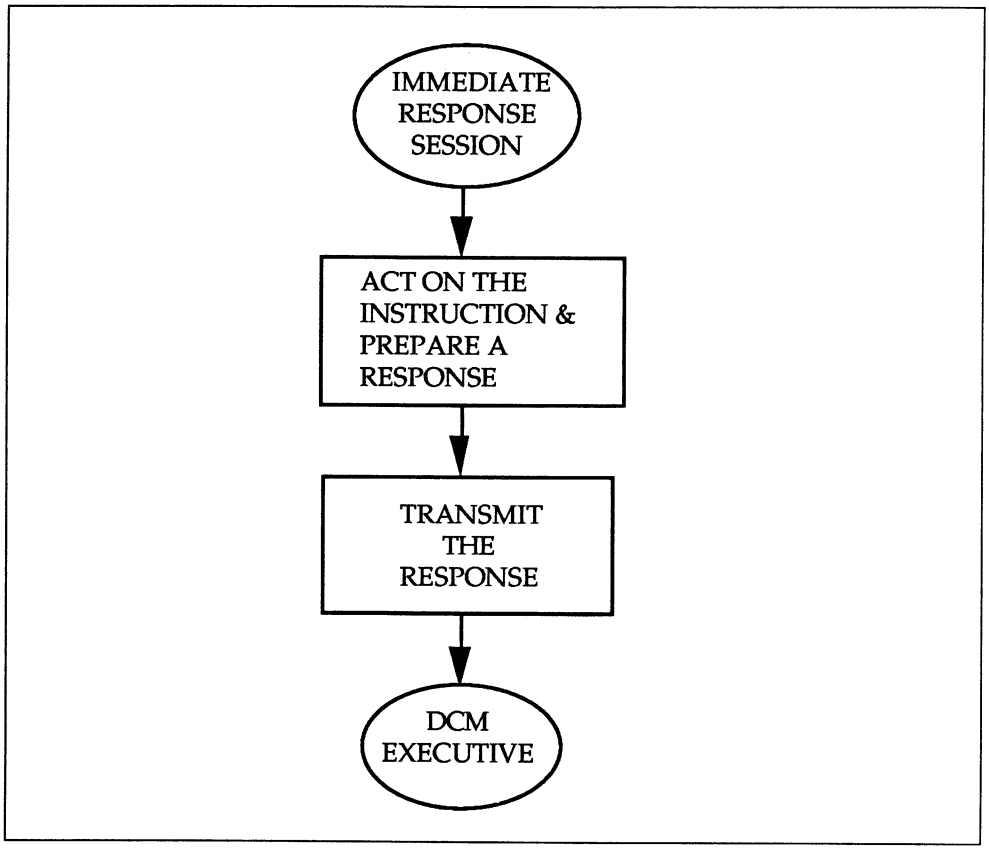


Continued on next page

Immediate response session, continued

During the immediate response session, the DCM receiver is disabled (except during the response transmission if in the half-duplex mode, or during reception of a second valid message – see Figure 4-6).

Figure 4-6 Immediate Response Session

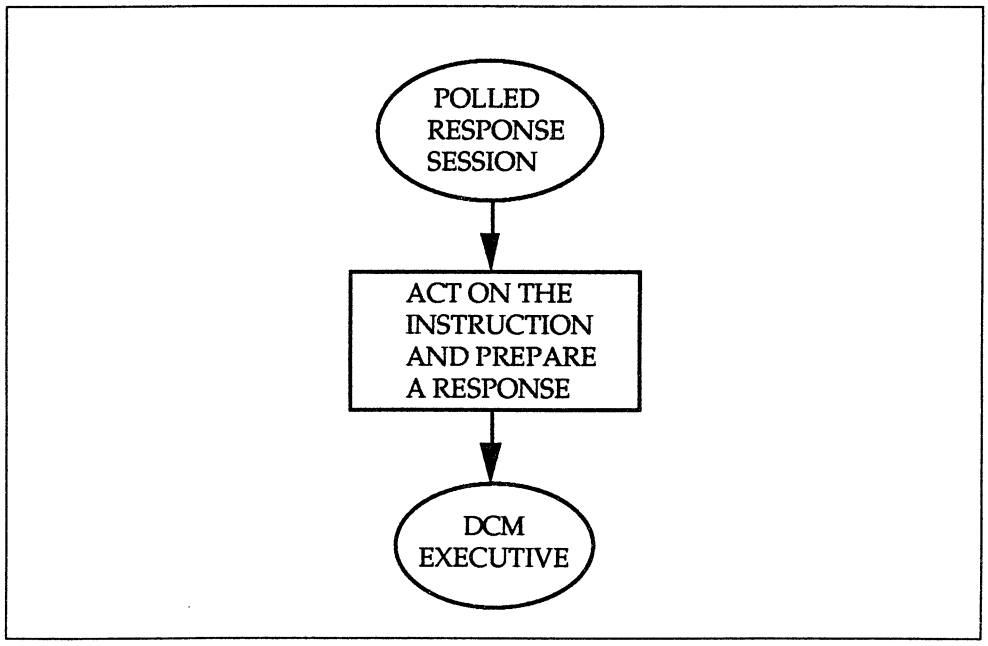


Continued on next page

Polled response session without acknowledge

During the polled response session without immediate acknowledge, the DCM receiver is enabled until a valid message is received (see Figure 4-7). This procedure has the same result as a polled response with acknowledge with the exception that an acknowledge response is not returned.

Figure 4-7 Polled Response Session Without Acknowledge



Continued on next page

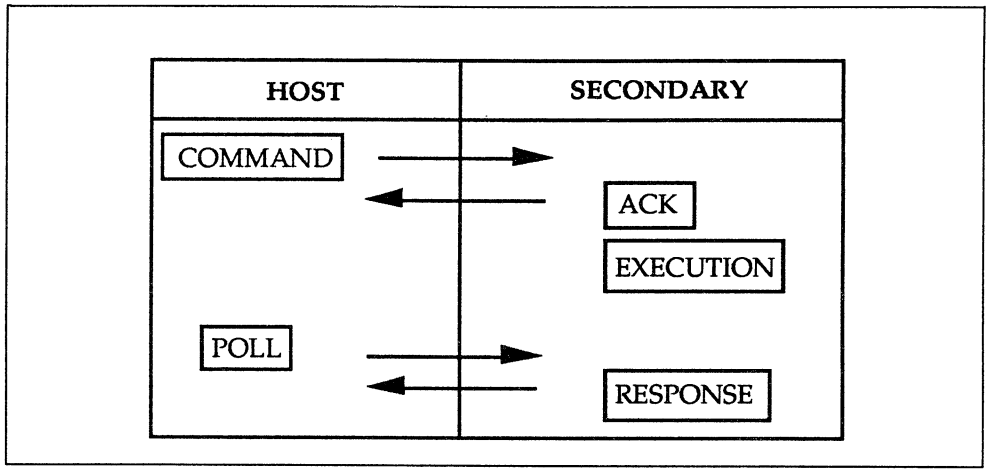
Polled response session with acknowledge

With the polled response with acknowledge procedure, the host issues a command message that includes an ACK request. If the secondary receives a valid command, it sends an acknowledgement response and executes the command.

The response is held in the secondary's transmit buffer until the host polls for it. If the host issues a poll command before the secondary has finished the command execution, the host must wait for the secondary to respond with the result. Fail-safe timeout delays within the host are short for the ACK response, but depend on the command issued for polled responses (see Figure 4-8).

During the polled response session, the DCM receiver is enabled until a valid message is received (see Figure 4-8).

Figure 4-8 Polled Response Diagram

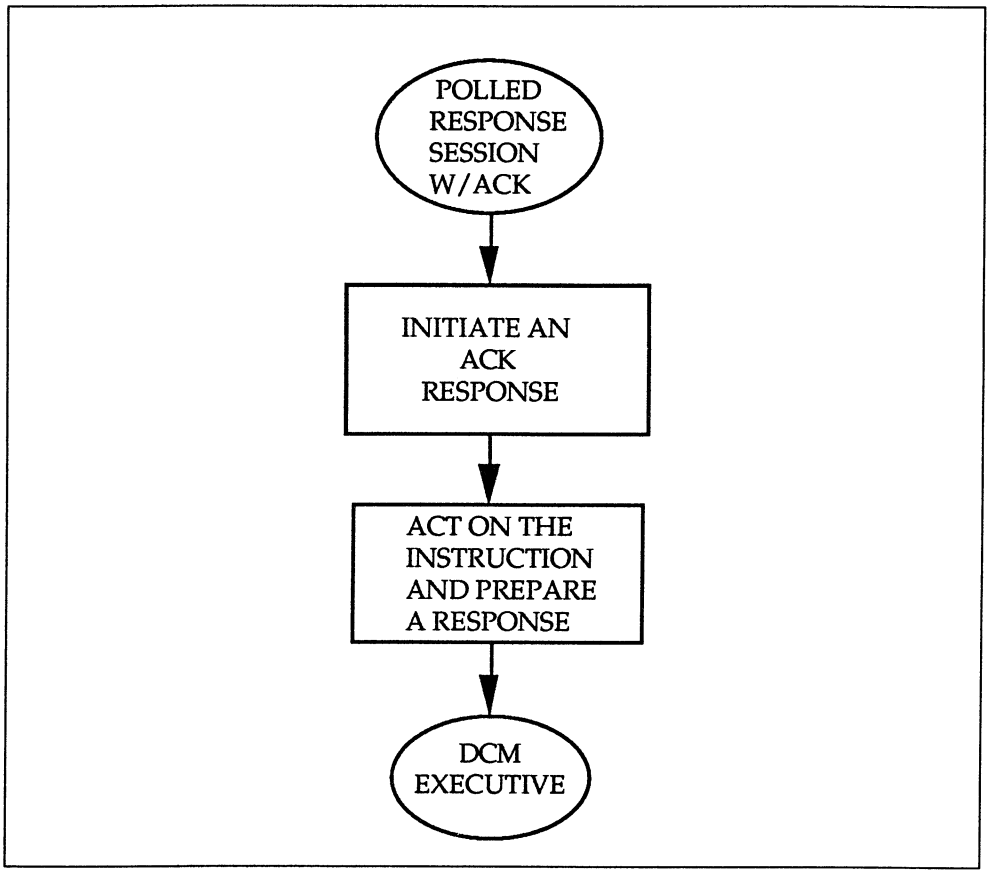


Continued on next page

Polled response session with acknowledge, continued

During the polled response session with immediate acknowledge, the DCM receiver is enabled until a valid message is received (see Figure 4-9).

Figure 4-9 Polled Response Session With Acknowledge

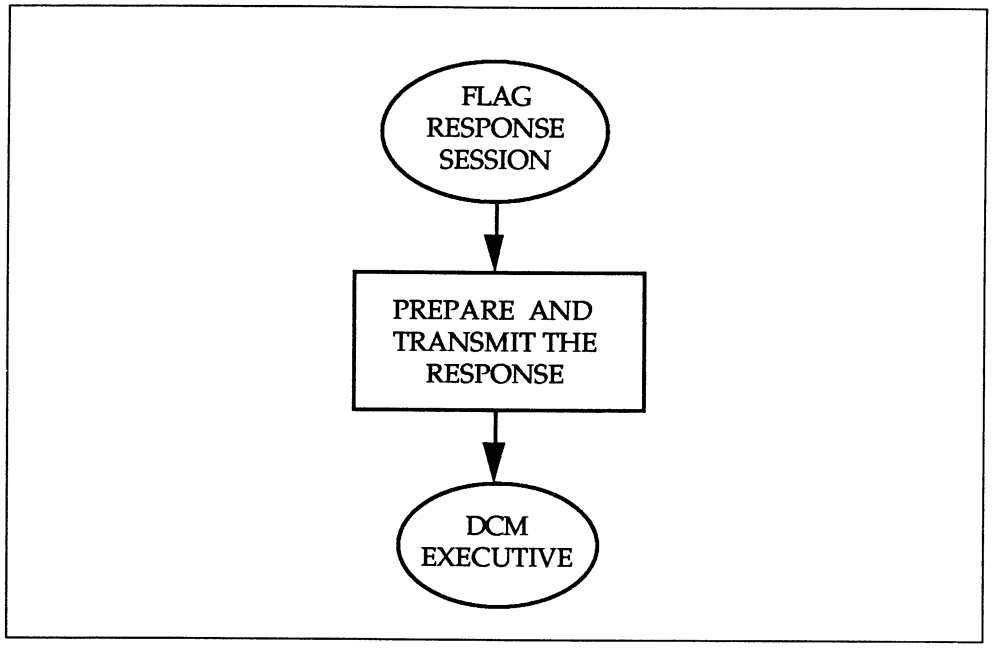


Continued on next page

Flag response session

During the flag response session the DCM receiver is enabled until a valid message is received (see Figure 4-10). The flag response is initiated by the secondary when a change in status of predefined control bits occurs within the secondary station. The host gives no preceding command or subsequent acknowledgement.

Figure 4-10 Flag Response Session



ATTENTION

ATTENTION: Refer to *Flag Mode Operation* for more information on the flag mode.

Flag Mode Operation

Background

The flag mode is a DIP switch-selectable alternative mode of operation. It allows the DCM to provide data to the host without the host requesting it. This data exchange occurs when specific control relays within the processor change from an OFF to ON state.

Conditions for flag mode operation

The following conditions must be met for flag mode operation:

- flag mode operation must be enabled by the DIP switch selections (refer to Section 3),
- point-to-point serial port configuration must be selected. A direct connect full-duplex connection is necessary with either RS232 or RS422/485, and
- the DCM's applicable port must not be in the data collection mode.

Flag mode function

The flag mode function extends the DCM's monitoring functions to include the sixteen most significant bits of the processor's output status table. The DCMs read specified flag bits at the beginning of the LCS's program memory scan. Refer to Table 4-6 for the specified flag bits used by each 620 LCS. Refer to Section 5 for the flag mode response format.

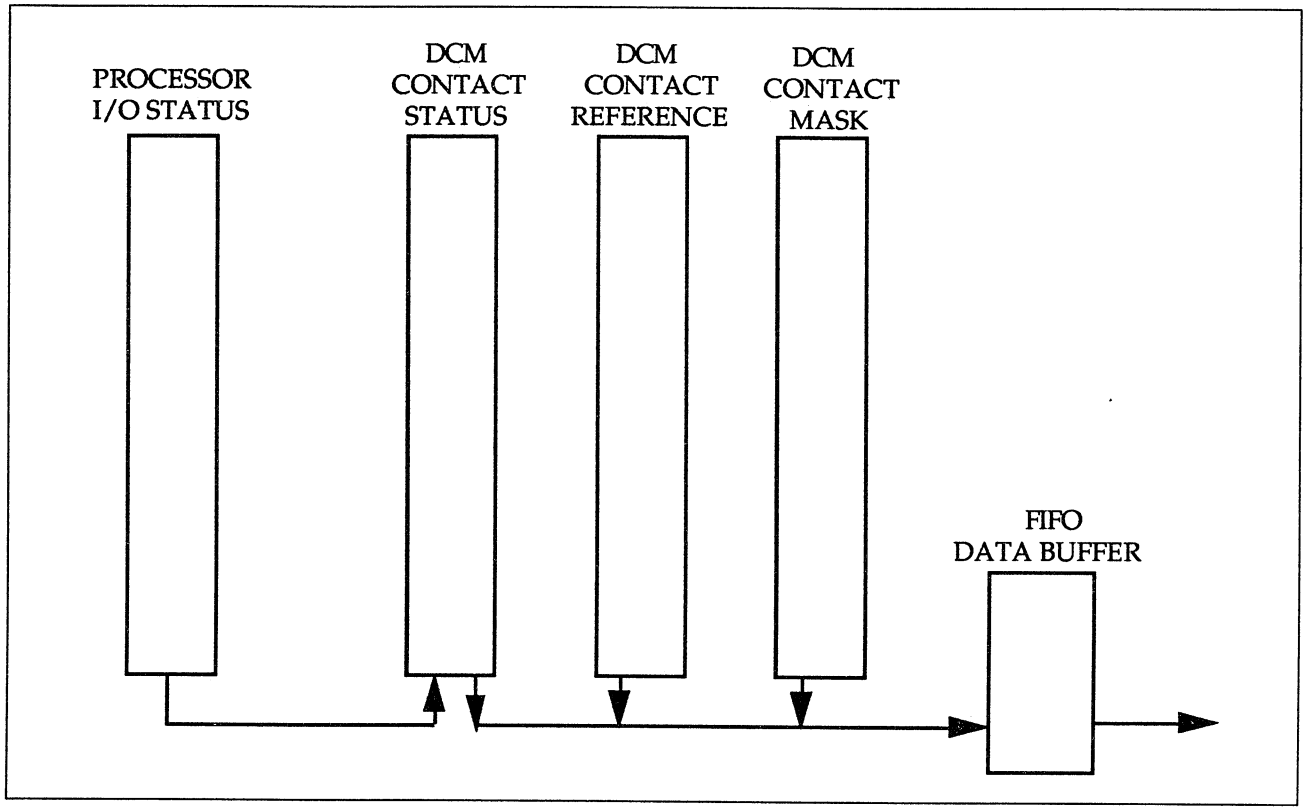
Table 4-6 Flag Bits Used in 620 LCSs

620 LCS	Flag Bits
620-06/10/15	DCM reads bits 752 to 767 as flag bits.
620-11/12/14/1631/1633/36	Flag bit range is programmable in these processors through a Modify Flag Mode routine; you can write to addresses 2501 (least significant byte) and 2502 (most significant byte) in the System Status Table (or use the auxiliary menu on the 623-60 MS-DOS Loader/Terminal) to specify the most significant address of the desired range of flag bits. Otherwise, the processor defaults the flag bit range to addresses 2016 to 2031 and DCM monitors these addresses for OFF-to-ON transitions.
620-20/25/30/35	DCM reads bits 2032 to 2047 as flag bits; if an OFF-to-ON transition has occurred since the last read, a response is prepared and transmitted to the host.

DCM I/O status tables

Refer to Figure 4-11 for a presentation of the DCM I/O status tables — the Contact Status Table, the Contact Reference Table, and the Contact Mask Table.

Figure 4-11 DCM I/O Status Tables



Continued on next page

DCM contact reference table

While in the data collection mode, the DCM copies part of the I/O Status Tables at the end of each processor scan. The data is placed in the Contact Reference Table and is used for comparisons to determine if contacts have changed.

DCM contact status table

The Contact Status Table is filled after the Contact Reference Table. The DCM compares the data in the two tables and determines which contacts have changed status. The contacts are then compared with the Contact Mask Table.

DCM contact mask table

The Contact Mask Table holds user-specified addresses to be excluded from the data collection process. These addresses must be within the data collection range. Addresses of contacts that have changed status and have not been masked by this table are placed in the FIFO buffer.

FIFO buffer

The FIFO buffer stores a time tag along with addresses of changed contacts. It is a reference for the time when the contact status changed. A time tag is calculated and stored in the FIFO buffer at the beginning of each comparison of the Contact Reference Table and the Contact Status Table.

Time tags

The time tags are derived from a binary count of the number of 100 ms intervals starting at the beginning of data collection. The average scan time of the processor is used as a time base for calculating time tags. The DCM reads the scan time from the processor System Status Table during each backplane window. Also, the DCM keeps a running total of the average scan times.

Every time the total accumulates another 100 ms, the count is incremented by 1 and stored in the FIFO buffer. The last time tag in the FIFO buffer is continuously overwritten until new contact status changes occur. This prevents the FIFO buffer from filling up with time tags.

The time tags are a relative time reference and only have meaning in relation to previous time tags. They may be used to determine how much time has passed since the last time tag was posted.

Continued on next page

Average scan times

At cold start (when power is first applied to the processor), data collection does not begin until an average scan time is established for the LCS. The following number of scans are required for each respective LCS to establish an average scan time:

- For 620-06/10/15 LCSs — 52 scans
- For 620-11/14/16 LCSs — 10 scans
- For 620-12/1633/36 LCSs — 10 scans
- For 620-20/25/30/35 LCSs — 12 scans

Data collection

After the DCM has compared all the data in the Contact Reference and Contact Mask Tables, the Contact Reference Table becomes free for new I/O information. The Contact Reference and Contact Status Tables then become filled sequentially, with the present Contact Status Table becoming the Contact Reference Table for the next comparison.

The entries in the FIFO buffer show the history of the processor's I/O operation. The buffer holds 1024 contact status and time tag entries.

ATTENTION

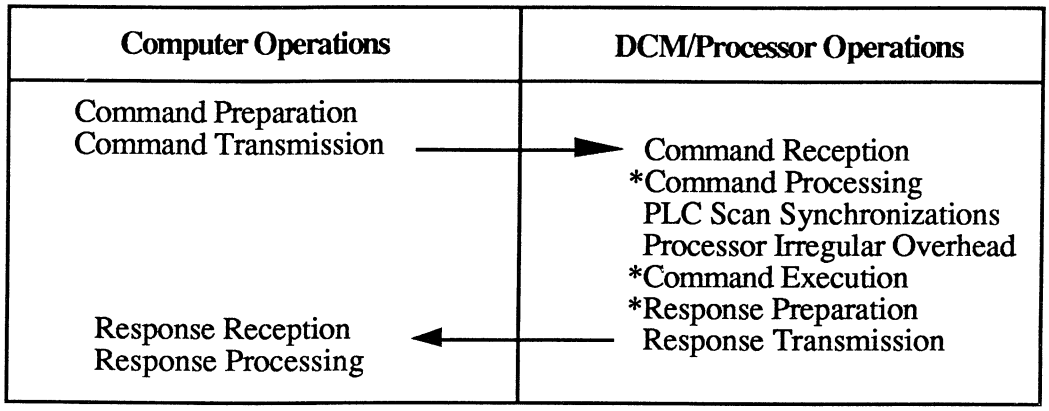
ATTENTION: Data can be collected through the 620-0048 DCM port and port 1 of the 620-0052 DCM. An invalid opcode error message occurs if data collection instructions are sent to port 2 of the 620-0052 DCM.

Session Execution Time

Total exchange time

Refer to Figure 4-12 and Table 4-7 for the operations in session execution time; refer to Table 5-5 for a list of instruction execution times in milliseconds. To calculate the total exchange times, add the times required by these operations (that is, total exchange time is the sum of the times required by the operations listed in Figure 4-12). This time frame extends from the host computer's decision to acquire certain information until the data is in the computer's data base.

Figure 4-12 Operations in Session Execution Time



* These operations are performed during time slots granted by the processor.

Continued on next page

Total exchange time, continued

Table 4-7 Descriptions of Operations in Session Execution Time

Operation	Description
Command Preparation Response Preparation	Time for these operations is a function of the host computer.
Command/Response Reception Command/Response Transmission	Time for these operations is a function of the baud rate and message size according to the following formula: **Transmission time in milliseconds =** **No. bits per character x baud rate** **No. characters x 1000**
Command Processing Response Preparation	Time for these operations varies slightly with each instruction — assume 0.5 milliseconds.
Processor Scan Synchronization	This time is required when instructions require data exchanges with the processor. This is the time that elapses while the DCM waits for its data exchange window at the beginning of each scan (Memory Word Zero). The time is less than 2ms if the processor is in the PROGRAM mode, or potentially equal to processor scan time if the processor is in the RUN mode. The processor maintains a record of its average scan time in the System Status Table. To access the scan time record, use the "Read 1 Status Register" instruction with a starting address of decimal 2291. The result is an 8-bit binary number representing the average scan time in milliseconds.

Continued on next page

Total exchange time, continued

Table 4-7 Descriptions of Operations in Session Execution Time, continued

Operation	Description
Processor Irregular Overhead	This time is the result of external stimuli, such as other DCMs, the processor Loader/Terminal, or the processor keyswitch, which extend processor scan time between DCM access windows. The Loader/Terminal can add up to 300ms to a scan, and each DCM can add up to: • 40 ms in a 620-06/10/15/20/25/30/35 processor, • 90 ms in a 620-11/14/16 processor, and • 90 ms in a 620-12/1633/36 processor. If the processor is switched from PROGRAM to RUN mode, the DCM is denied access during processor diagnostics, which required approximately 650 ms plus one scan time.
DCM/Processor Data Exchange	This is the time required by the DCM to execute the exchange once it receives a window. Refer to Table 5-5 for the time for this operation.

Error Recovery

Erroneous secondary receptions

Any errors generated during message reception result in no action by the secondary. The error situation is detected by the host through its timeout mechanisms. Retransmission is a host decision.

Host reception of erroneous information messages

The host has three options after receiving an erroneous secondary response:

- retransmit the command,
- poll for a (re)transmission of the response, or
- abort the exchange.

Host reception of erroneous flag responses

The host has two options following the reception of an erroneous flag response:

- poll for a (re)transmission of the response, or
- ignore the message.

Host reception of erroneous acknowledgements

The host has two options after receiving an erroneous acknowledgement:

- retransmit the command, or
- ignore the ACK (that is, the host assumes that the erroneous acknowledgement should have been an ACK and not a flag response or an ACK from another station. This is a valid assumption in a point-to-point system with the flag mode disabled).

DCM Program Memory Checksum

Background

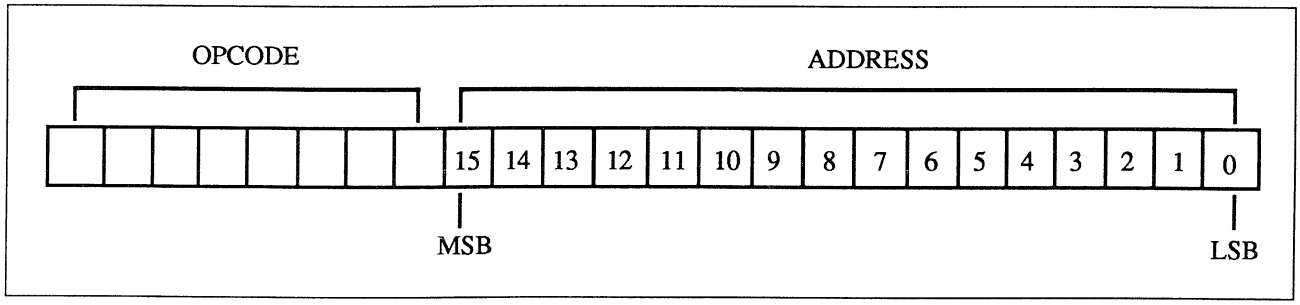
The DCM performs a checksum of the host processor's program memory (refer to Figure 4-13 for a description of the 620 LCS program memory word organization). The checksum is a 16-bit binary value of each user memory word, including the Input Status Scan (ISS) and End of Memory (EOM) instructions. The history and force bits associated with each opcode are masked off, so the checksum calculation is not affected by forced contacts and opcodes that use history bits. However, if a Load Sequencer instruction is programmed and executed, the checksum routine flags an error and is updated to include the Load Sequencer.

The DCM stores the results of the checksum calculation, error flag, error history flag, and initial pass flag in the host processor's System Status Table. You may use the flags as inputs to the processor program to control I/O in the event of an error. The DCM Read System Status Registers instruction can read the checksum data from the host.

The program memory checksum calculation is performed while the host processor is in the DISABLE, RUN/PROGRAM, or RUN mode. The checksum routine is disabled when the host is switched to the PROGRAM mode or software PROGRAM mode.

Only the DCM at backplane address 0 performs the checksum calculation if more than one DCM is being used.

Figure 4-13 620 LCS Program Memory Word Organization



Continued on next page

DCM Program Memory Checksum, Continued

Checksum operation

The checksum routine clears the initial pass flag and the checksum register when the host processor is switched from PROGRAM to any of the RUN modes. The error history flag and error flag are set to 128 to indicate a pass condition. The checksum routine adds one user memory word per scan starting with the ISS instruction to the temporary checksum register until the EOM is reached. When the EOM is reached, it is added to the temporary checksum register, and the temporary checksum register is transferred to the System Status Table of the host processor. The initial pass flag is set to 128 to indicate the initial pass is complete.

The checksum routine again starts at the ISS instruction and starts a second pass. Each time the pass is complete, the new checksum value is compared with the last checksum value. If the checksum values equate, the error flag is set to indicate that the present pass is the same as the prior. If the two values do not equate, the error flag is cleared to indicate that the checksum value has changed, and the new checksum value is transferred to the host. The routine continues to calculate the checksum of user memory until the host is switched to the PROGRAM mode.

Checksum execution time

The checksum routine adds one memory word per scan. The execution time of one checksum pass can be calculated by multiplying the number of program words by the average scan time.

Continued on next page

Checksum flags and registers

The checksum routine uses five bytes of the System Status Table in the host processor to store the results of the checksum calculation. Refer to Table 4-8 for descriptions of how each allocated System Status Table address is used for the checksum routine.

Table 4-8 Checksum Flags and Registers

System Status Table Address	Description
Address 2384 – Checksum Low Byte	This address is the least significant byte of the checksum calculation.
Address 2385 – Checksum High Byte	This address is the most significant byte of the checksum calculation.
Address 2386 – Error Flag	The error flag indicates that the checksum value has changed since the last pass of user memory. The error flag set at 128 indicates that the checksum has not changed since the last pass of user memory. This address set at 0 indicates that the checksum value has changed since the last pass of user memory.
Address 2387 – Error History Flag	The error history flag indicates that the checksum calculation has changed after the initial pass is complete. The error history flag, if set at 128, indicates that the checksum has not changed; if set at 0, indicates that the checksum has changed since the initial pass.
Address 2388 – Initial Pass Flag	The inital pass flag indicates that the checksum routine has made a complete pass of user memory. The routine reads one user memory word per processor scan and adds each word to the checksum register. When the EOM opcode is reached, it is added to the temporary checksum register. The temporary checksum register is transferred to the host processor status table and the initial pass flag is set to 128 to indicate a valid checksum has been calculated.

Section 5 – DCM Instruction Set

Overview

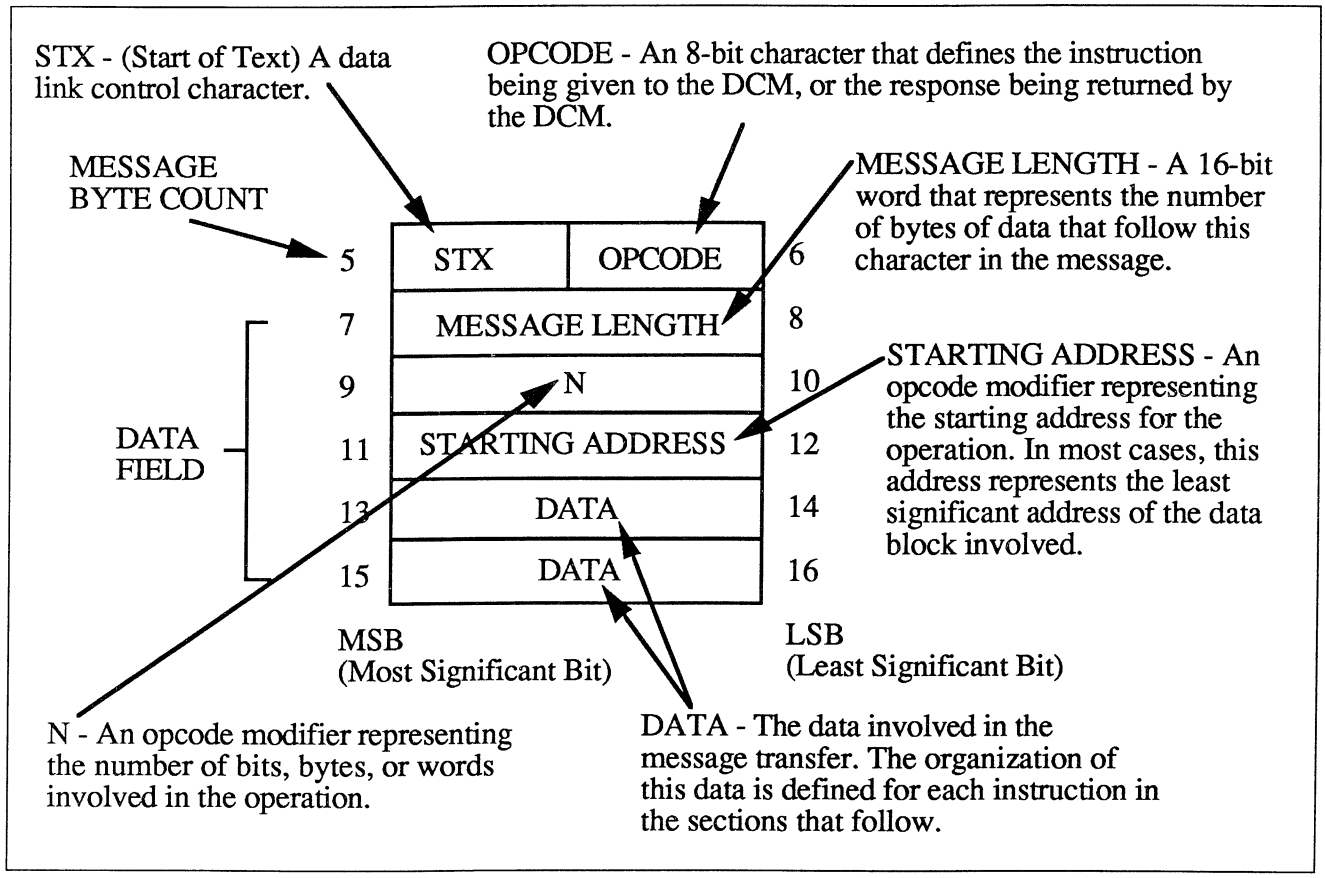
Section contents

Continued on next page

DCM instructions and opcodes

Refer to Table 5-1 (next page) for the instructions and function codes that the DCM is programmed to recognize. The individual descriptions that follow are separated into functional categories. Each actual instruction description includes title, definition, and instruction and response message formats. Only the text portion of the message format is provided. Refer to Figure 5-1 for descriptions of the various characters used in the text. Refer to the Figure 4-4 for total message format and to Table 5-5 for instruction execution times.

Figure 5-1 General Message Text Structure for 620-0048/0052 DCMs



Continued on next page

DCM instructions and opcodes, continued

Table 5-1 DCM Instructions and Opcodes

Opcode (Decimal)	Instruction
	Input/Output Instructions
02	Read 16N I/O
20	Read 16N Scattered I/O
12	Write N Outputs
14	Write 16N Outputs
24	Write N Scattered Outputs
	Data Collection Instructions
82	Initiate Data Collection
84	Terminate Data Collection
86	Read Data Buffer
88	Read Mask Table
90	Read Reference Table
92	Write Mask Table
94	Inhibit Mask Table
96	Enable Mask Table
	Register Instructions
04	Read N Registers, No Sign
06	Read N Signed Registers
22	Read N Scattered Registers
16	Write N Registers, No Sign
18	Write N Signed Registers
26	Write N Scattered Registers
28	Pull N I/O Registers
30	Push N I/O Registers
08	Read N System Status Registers
10	Write N System Status Registers
	620 LCS Processor Control Instructions
52	Request PROGRAM Mode
54	Remove PROGRAM Mode Request
76	Write I/O Configuration
78	Write Processor Control Configuration
	Program Memory Instructions
34	Upload N Program Memory Words
36	Download N Program Memory Words
38	Clear Program Memory
40	Insert N Program Memory Words
42	Delete N Program Memory Words
	Program Header Instructions
64	Upload Program Date
66	Upload Programmer
68	Upload Title
70	Download Program Date
72	Download Programmer
74	Download Title
	Diagnostic Instructions
0	Read DCM Status
80	Loop Back Test

M and L values for 620 CPMs

For DCM instructions presented in this section, the variable M represents the highest starting address available. The value of M depends on the type of 620 Control Processor Module (CPM), its memory configuration, and the type of memory accessed. The variable L represents the highest real I/O address available. The value of L depends on the type of 620 CPM. Refer to Table 5-2 for M and L values for the various 620 CPMs.

Table 5-2 M and L Values for 620 CPMs

620 CPM	Memory Size	M Value	L Value
620-0636	2K	4351	191
620-1034	1/2K	4351	255
620-1534	1/2K	4351	255
620-1035	1K	4351	255
620-1535	1K	4351	255
620-1036	2K	4607	511
620-1200	2K	4351	255
620-1536	2K	4607	511
620-1037	4K	4607	511
620-1537	4K	4607	511
620-1131	8K	8191	255
620-1431	8K	8191	639
620-1631	8K	8191	2039
620-1633	8K	8191	1023
620-3632	32K	8191	2039
620-20	2K Register	6143	511
620-25	2K Register	6143	2047
620-25	4K Register	8191	2047
620-30	2K Register	6143	2047
620-30	4K Register	8191	2047
620-35	2K Register	6143	2047
620-35	4K Register	8191	2047

Input/Output Instructions

Purpose of input/output instructions

Input/output instructions provide access to the ON/OFF status of individual or groups of addresses in the particular 620 LCS Input/Output Status Tables. READ I/O instructions obtain the status, and WRITE I/O instructions set the status.

The response to a successful READ I/O instruction is the logical "OR" of the input and output status locations asked for in the READ I/O instruction. The response to a successful WRITE I/O instruction is an acknowledgement that the write was successful.

Continued on next page

Read 16N I/O

This instruction reads the logical "OR" of N contiguous 16-bit address locations within the Input/Output Status Tables. Refer to Figure 5-2 for the instruction format and Figure 5-3 for the response format for this instruction.

Figure 5-2 Read 16N I/O Instruction Format

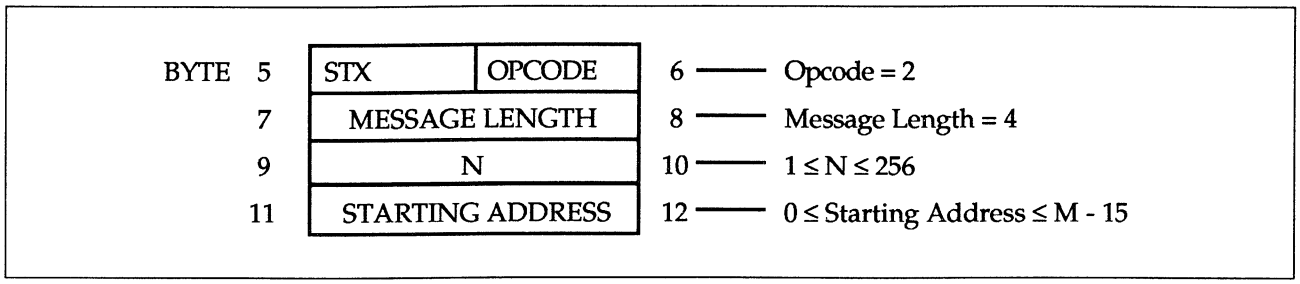
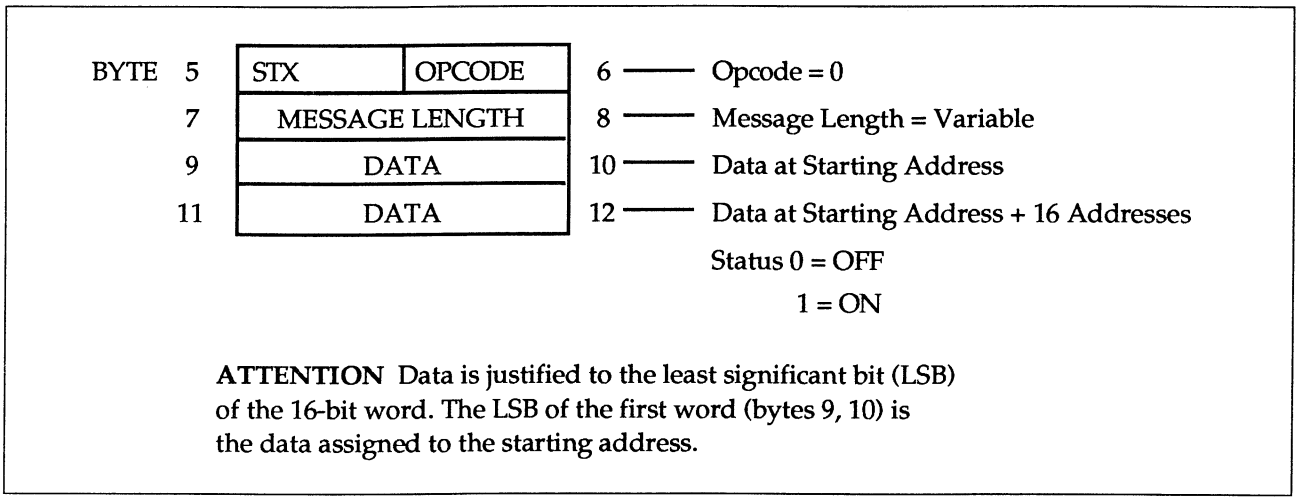


Figure 5-3 Read 16N I/O Response Format (Instruction Executed)



ATTENTION Data is justified to the least significant bit (LSB) of the 16-bit word. The LSB of the first word (bytes 9, 10) is the data assigned to the starting address.

Continued on next page

Read 16N scattered I/O

This instruction reads the logical "OR" of 16-bit groups of input/output addresses at various locations within the Input/Output Status Tables and control relay memory areas. Refer to Figure 5-4 for the instruction format and Figure 5-5 for the response format for this instruction.

Figure 5-4 Read 16N Scattered I/O Instruction Format

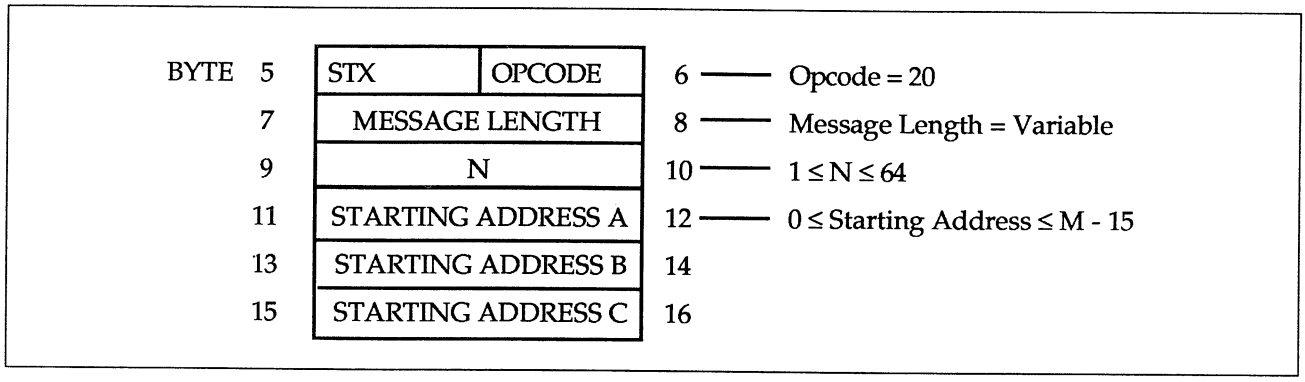
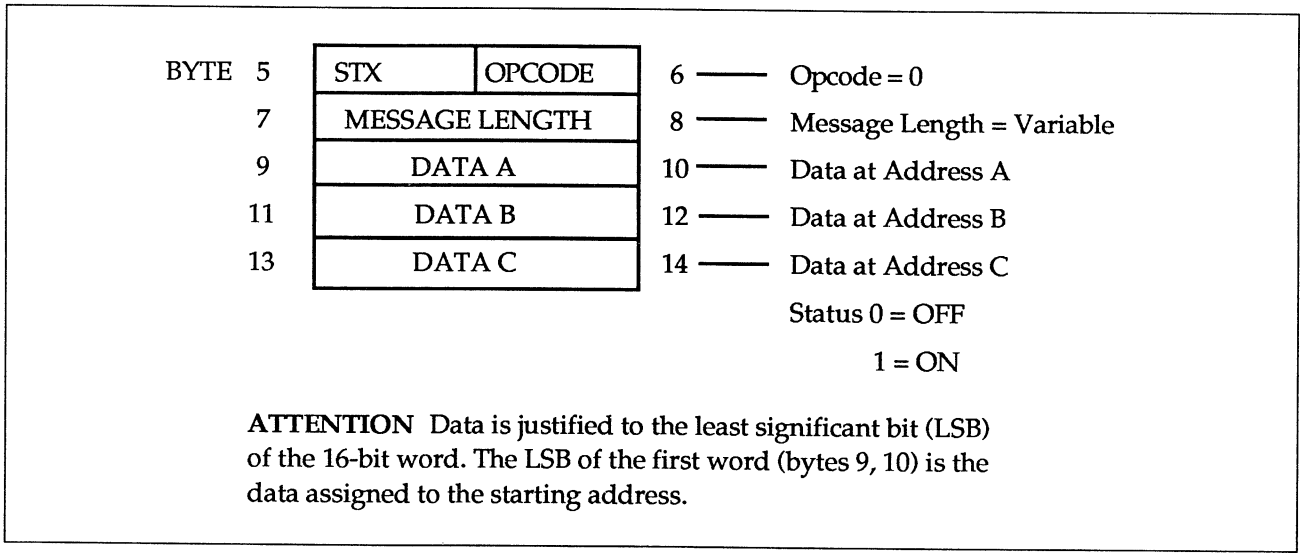


Figure 5-5 Read 16N Scattered I/O Response Format (Instruction Executed)



ATTENTION Data is justified to the least significant bit (LSB) of the 16-bit word. The LSB of the first word (bytes 9, 10) is the data assigned to the starting address.

Continued on next page

Write N outputs

This instruction writes N contiguous individual address locations in the Output Status Table and the real outputs. Refer to Figure 5-6 for the instruction format and Figure 5-7 for the response format for this instruction.

ATTENTION The DCM output write protect function must be disabled to execute this instruction.

Figure 5-6 Write N Outputs Instruction Format

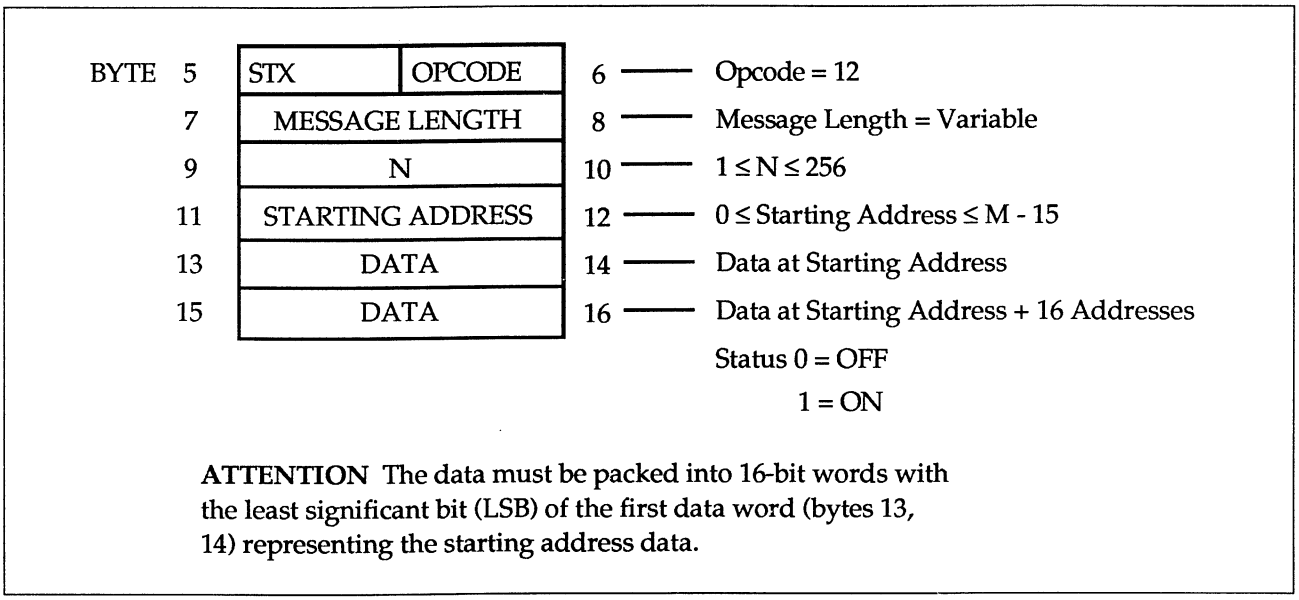
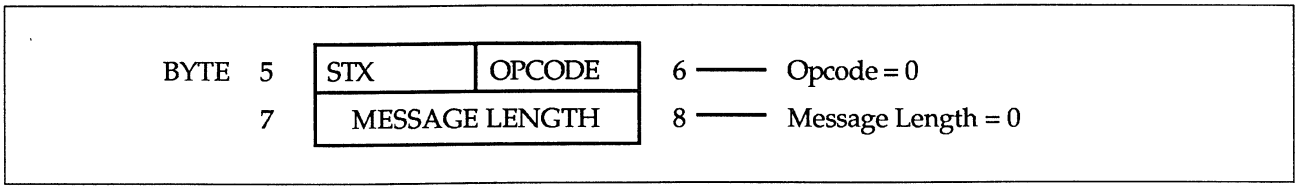


Figure 5-7 Write N Outputs Response Format (Instruction Executed)



Continued on next page

Write 16N outputs

This instruction writes N contiguous 16-bit blocks of address locations in the Output Status Table and the real outputs. Refer to Figure 5-8 for the instruction format and Figure 5-9 for the response format for this instruction.

ATTENTION The DCM output write protect function must be disabled to execute this instruction.

Figure 5-8 Write 16N Outputs Instruction Format

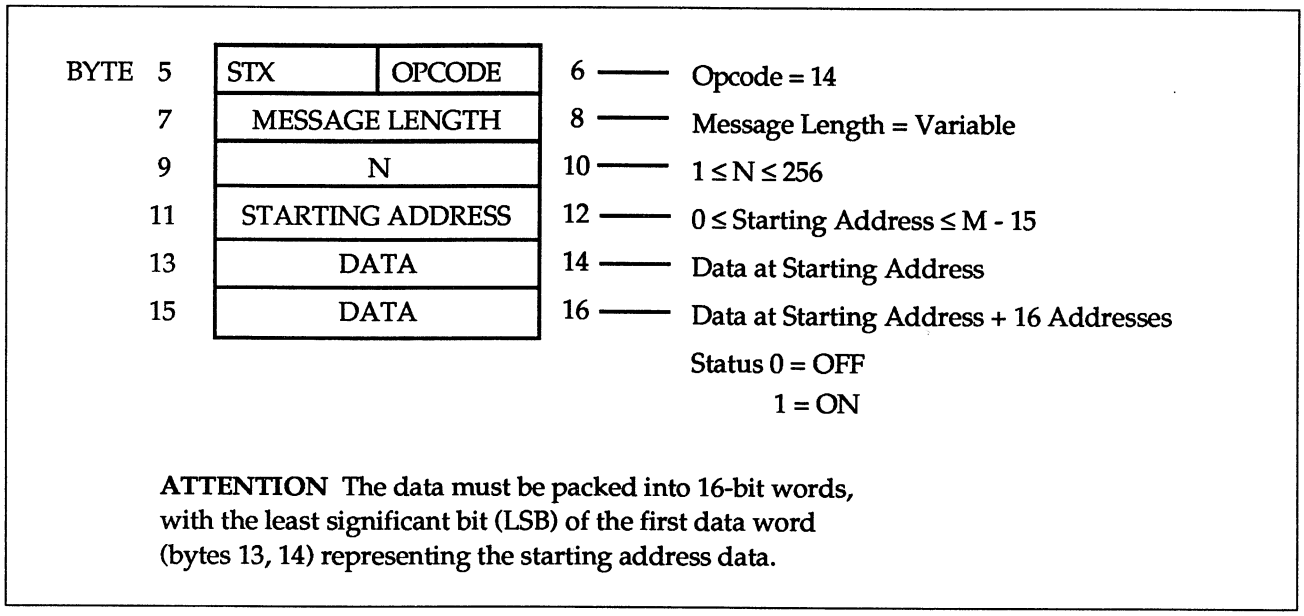
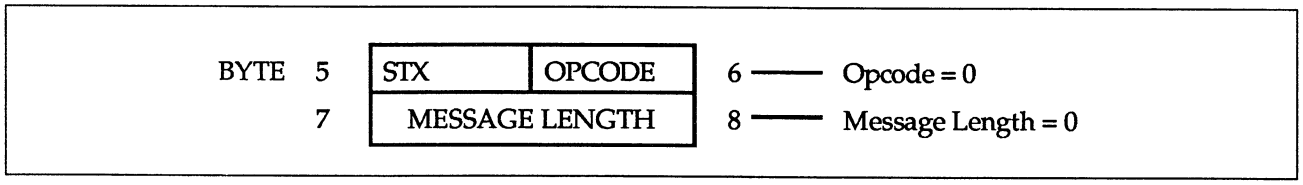


Figure 5-9 Write 16N Outputs Response Format (Instruction Executed)



Continued on next page

Write N scattered outputs

This instruction writes individual outputs at various locations that are not contiguous in the Output Status Table. Refer to Figure 5-10 for the instruction format and Figure 5-11 for the response format for this instruction.

ATTENTION The DCM output write protect function must be disabled to execute this instruction.

Figure 5-10 Write N Scattered Outputs Instruction Format

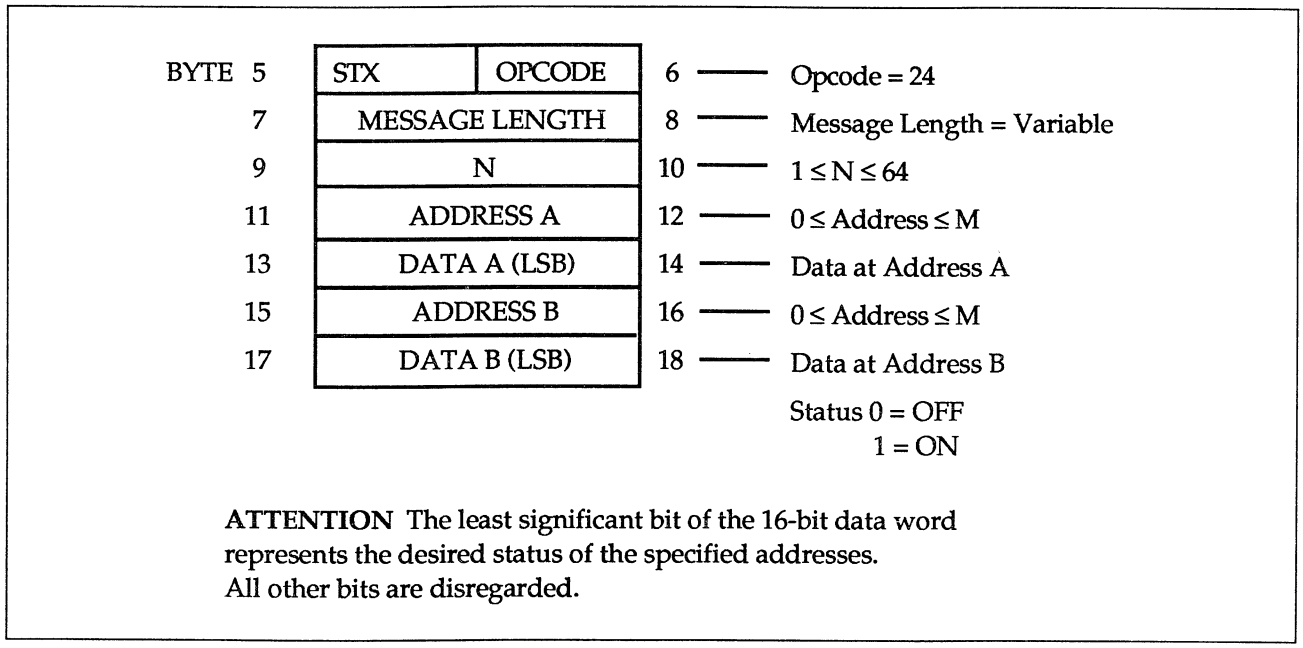
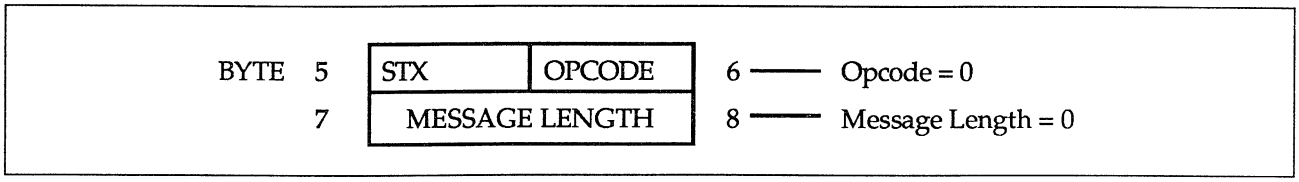


Figure 5-11 Write N Scattered Outputs Response Format (Instruction Executed)



Data Collection Instructions

Purpose of data collection instructions

Data collection instructions are used with the 620-0048 DCM and port 1 of the 620-0052 DCM to collect status information.

Continued on next page

Initiate data collection

The DCM begins to monitor the processor I/O Status Table when this instruction is received. If the status of any I/O location within the data collection range changes, the address and status are written into a FIFO buffer. Refer to Figure 5-12 for the instruction format and Figure 5-13 for the response format for this instruction.

ATTENTION The host processor must be in the RUN mode to execute this instruction. Flag mode operation is disabled when the DCM is executing data collection.

Figure 5-12 Initiate Data Collection Instruction Format

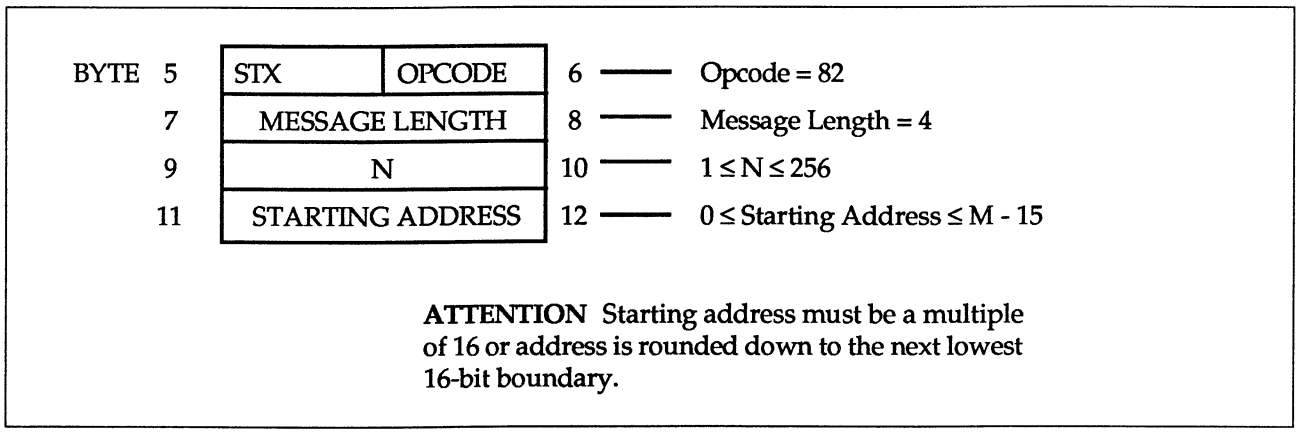
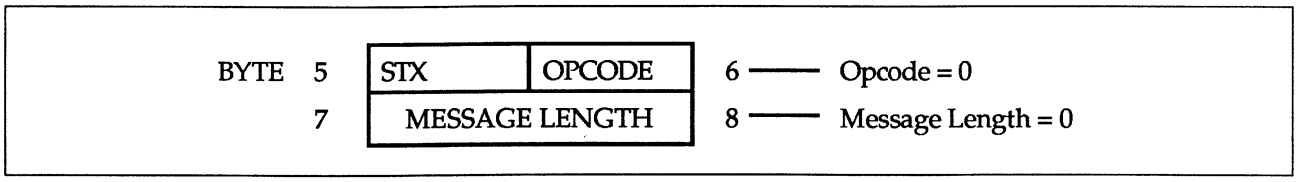


Figure 5-13 Initiate Data Collection Response Format (Data Collection in Progress)



Continued on next page

Terminate data collection

This instruction stops the DCM from monitoring the host processor I/O Status Table. Refer to Figure 5-14 for the instruction format and Figure 5-15 for the response format for this instruction.

ATTENTION If Flag mode is selected, it is reenabled when this instruction is initiated.

Figure 5-14 Terminate Data Collection Instruction Format

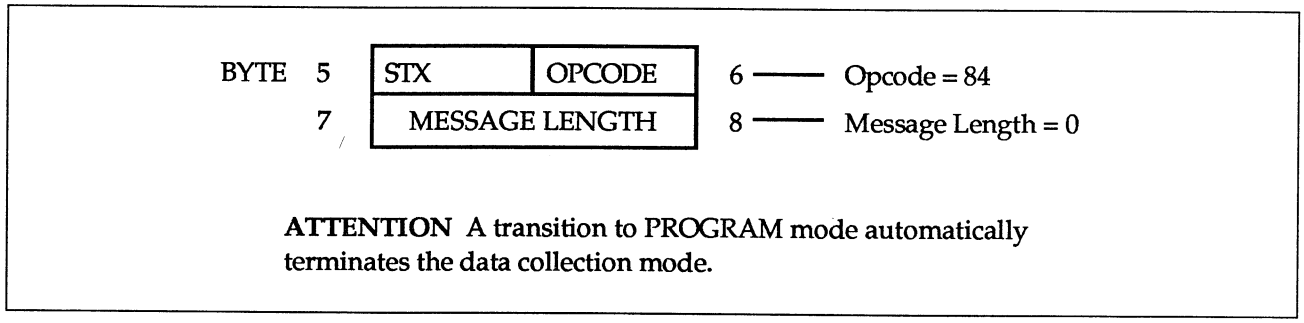
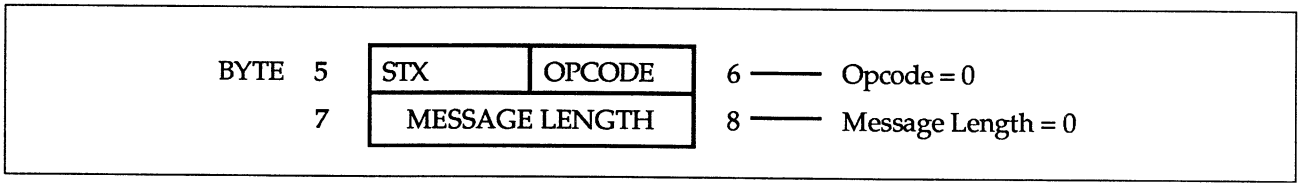


Figure 5-15 Terminate Data Collection Response Format (Instruction Executed)



Continued on next page

Read data buffer

This instruction reads up to 1024 entries from the FIFO buffer, which contains I/O status change information. Refer to Figure 5-16 for the instruction format and Figure 5-17 for the response format for this instruction.

ATTENTION

- Data collection does not have to be in progress to read the FIFO header. This allows the status byte in the FIFO header to be read to determine the status of the data collection process.
- Refer to Table 5-3 for status byte definitions for DCM read data buffer instructions.
- Refer to Figure 5-18 for the data format for the read data buffer instruction.

Figure 5-16 Read Data Buffer Instruction Format

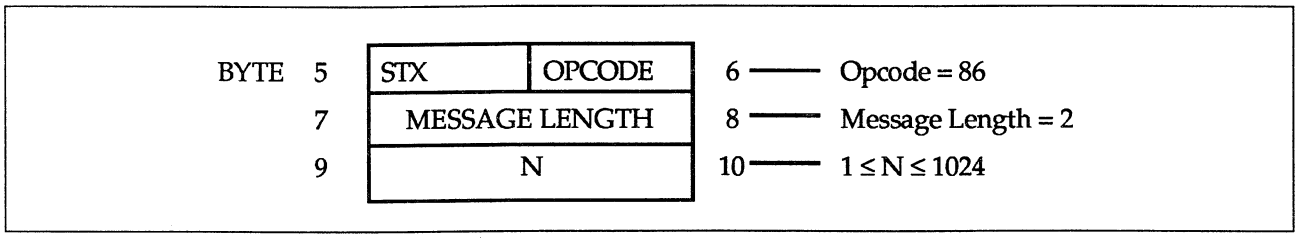
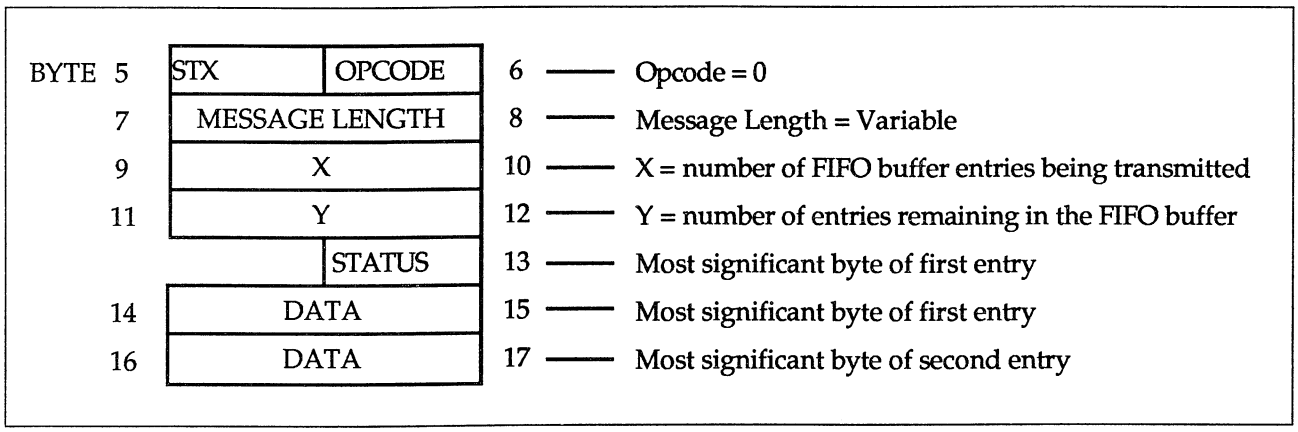


Figure 5-17 Read Data Buffer Response Format (Execution Acknowledge)



Continued on next page

Status byte for read data buffer

The status byte is used to determine the mode of the 620 CPM and if the data buffer or status table on the DCM is full. Also, one of the bits indicates if the DCM/620 CPM interface is functional. Refer to Table 5-3 for the definition of each bit.

Table 5-3 Status Byte Definitions for DCM Read Data Buffer Instructions

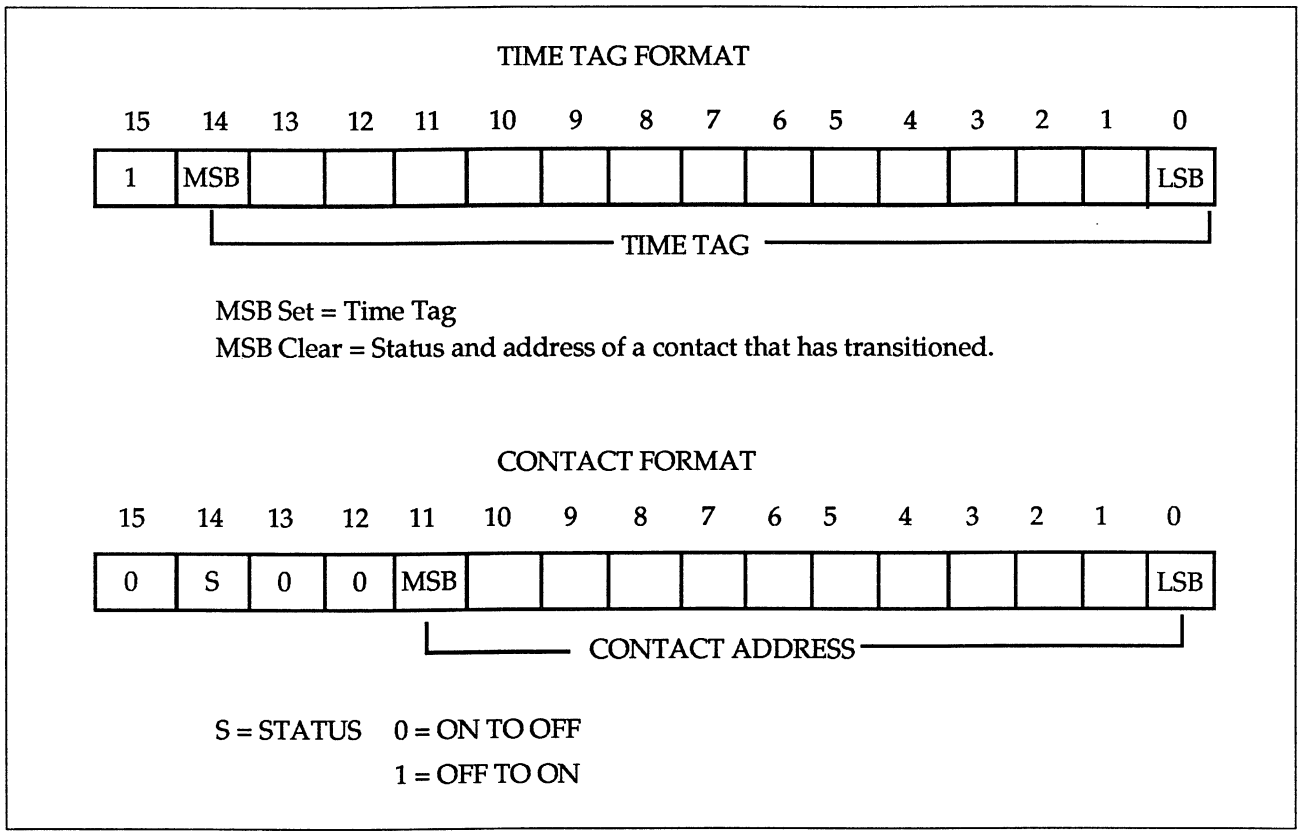
Bit	Function
0, 1, 2	Not used = 000.
3 Contact Status Overrun Bit	During memory word zero the DCM copies the 620 CPM's contact status table. A history table and a present table are maintained. When the processor starts scanning user memory, the DCM calculates the number of addresses of changed contacts in the table. The contact status overrun bit is set if the volume of I/O status changes is too great for the DCM to process. The bit is cleared when the read data buffer instruction is executed.
4 Data Buffer Overrun Bit	This bit is set when the DCM's FIFO buffer overflows (the DCM processes more I/O status changes than can be stored in the available space) and all entries prior to the overflow have been read. The bit is cleared when it is read.
5 Mode Transition Bit	This bit is set if the 620 CPM changes from the PROGRAM to RUN mode or from RUN to PROGRAM mode since the data buffer has been read last. The bit is cleared when it is read. Transitioning to PROGRAM mode terminates data collection.
6 Mode Bit	This bit indicates the mode of the processor. The bit is not cleared when read. 0 = PROGRAM, 1 = RUN. (PROGRAM mode terminates data collection).
7 Processor Interface Bit	This bit is set if the processor interface faults since the data buffer has been read last. The loss of the processor interface automatically terminates the data collection mode. The bit is cleared after it is read.

Continued on next page

Data format for read data buffer

The 16-bit data word is either a time tag or a transitioned contact. The most significant bit (MSB) of the data word indicates the type of data. Refer to Figure 5-18 for the data format for the read data buffer instruction.

Figure 5-18 Data Format for the Read Data Buffer Instruction



Continued on next page

Read mask table

This instruction reads the mask table in the DCM. The DCM reads up to 256 contiguous 16-bit blocks, beginning with the specified starting address. Refer to Figure 5-19 for the instruction format and Figure 5-20 for the response format for this instruction.

ATTENTION The starting address must be on a 16-bit boundary, or the address is rounded down to the next lowest 16-bit boundary.

Figure 5-19 Read Mask Table Instruction Format

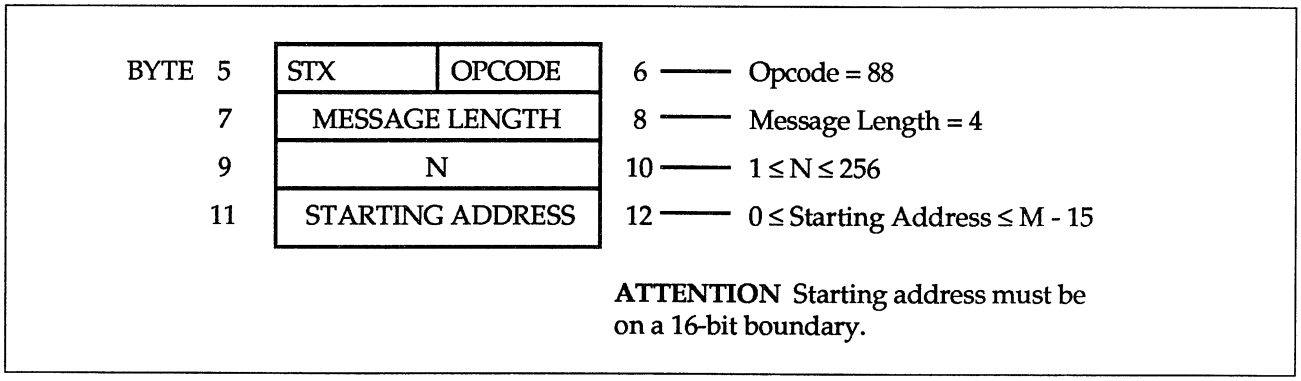
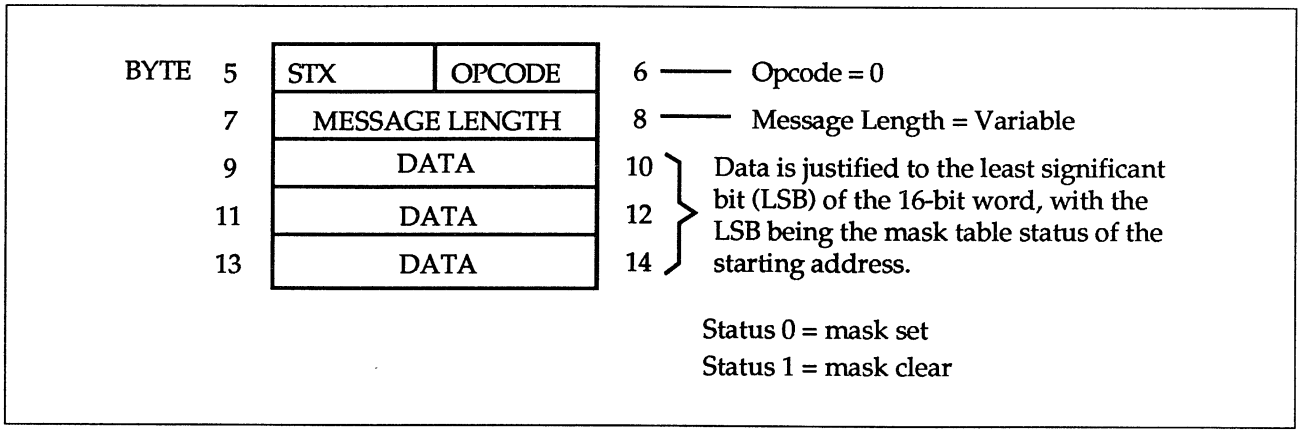


Figure 5-20 Read Mask Table Response Format (Instruction Executed)



Continued on next page

Read reference table

This instruction reads up to 256 contiguous 16-bit blocks of the I/O reference table in the DCM, beginning with the starting address. The data in the table is updated when the DCM is in the data collection mode. When data collection is terminated, the I/O status from the last update is retained in the reference table. Refer to Figure 5-21 for the instruction format and Figure 5-22 for the response format for this instruction.

ATTENTION The DCM must have its reference table initialized before it may be read. The starting address must be on a 16-bit boundary, or it will be rounded down to the next lowest 16-bit boundary. The DCM may not be in the data collection mode when executing this instruction.

Figure 5-21 Read Reference Table Instruction Format

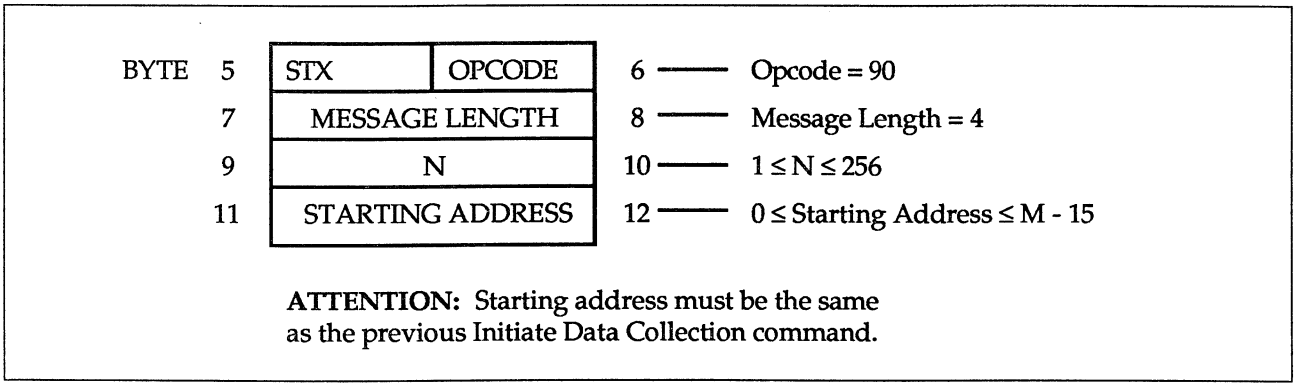
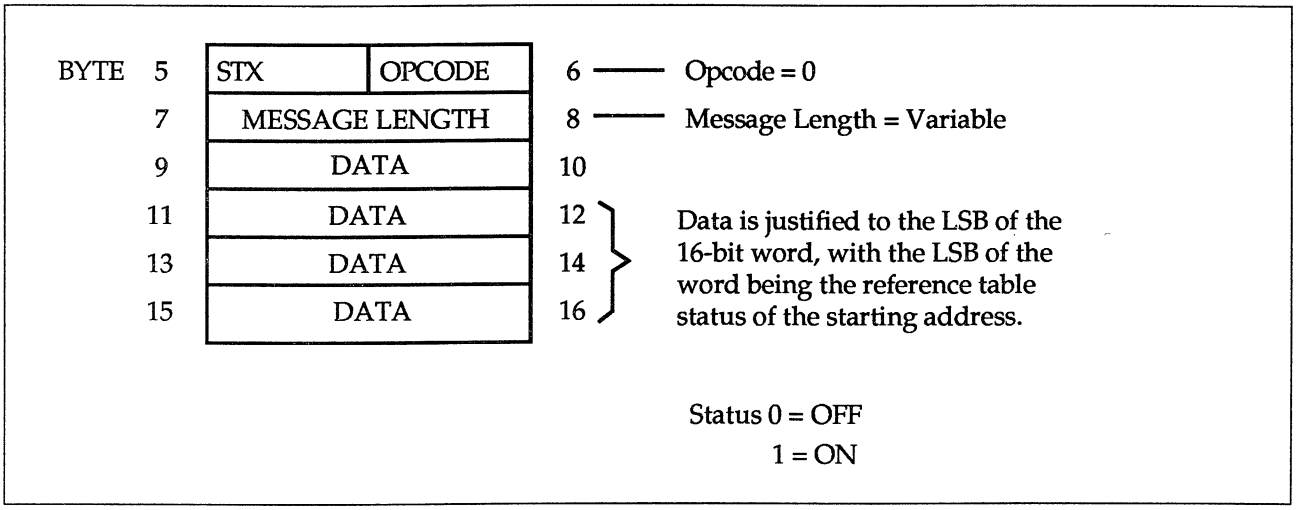


Figure 5-22 Read Reference Table Response Format (Instruction Executed)



Write mask table

This instruction writes to the mask table located in the DCM. The DCM writes 16N locations, beginning with the specified starting address and continuing upward. The starting address must be on a 16-bit boundary, or it will be rounded down to the next lowest 16-bit boundary. Refer to Figure 5-23 for the instruction format and Figure 5-24 for the response format for this instruction.

ATTENTION This instruction is necessary only if specific masking is desired. The DCM automatically sets all addresses to the unmasked state at power-up. This instruction may not be performed while the DCM is in the data collection mode.

Figure 5-23 Write Mask Table Instruction Format

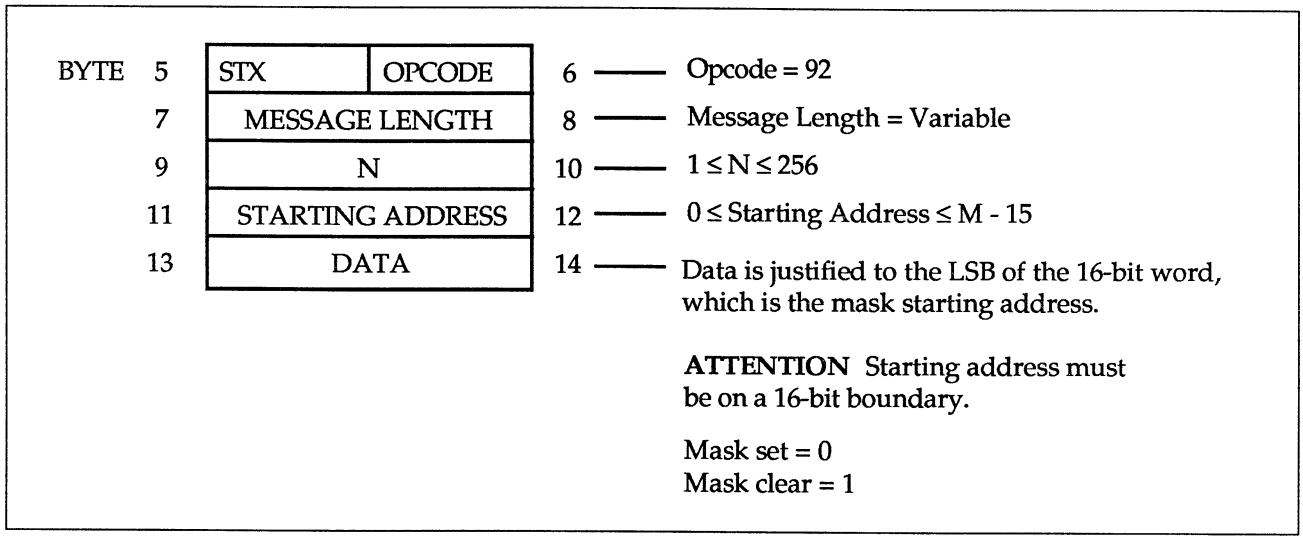
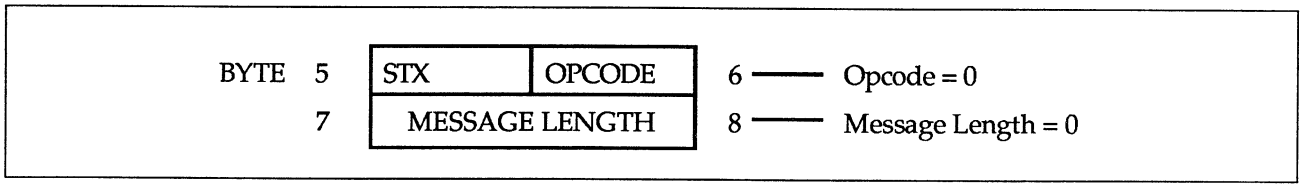


Figure 5-24 Write Mask Table Response Format (Instruction Executed)



Continued on next page

Inhibit mask table

This instruction prevents changing I/O locations from being masked during the data collection mode. Refer to Figure 5-25 for the instruction format and Figure 5-26 for the response format for this instruction.

Figure 5-25 Inhibit Mask Table Instruction Format

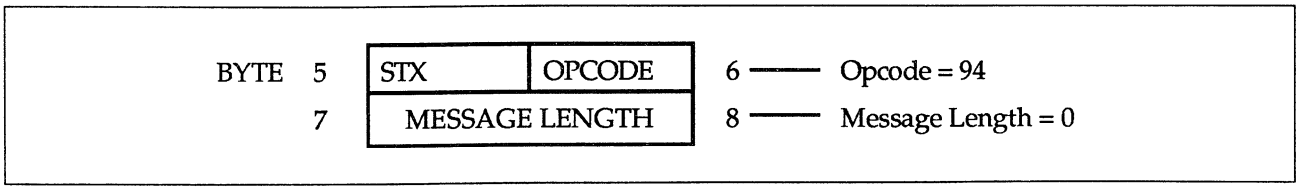
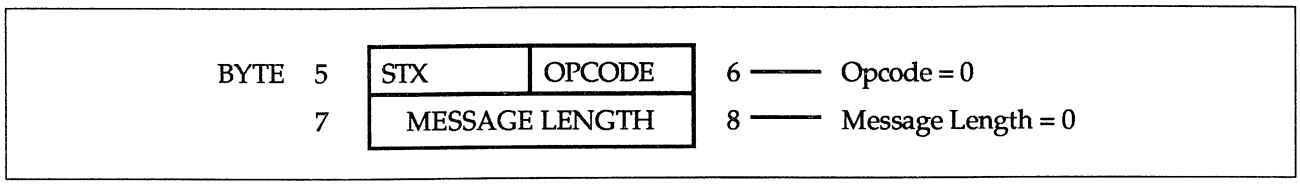


Figure 5-26 Inhibit Mask Table Response Format (Instruction Executed)



Continued on next page

Enable mask table

This instruction enables the mask table operation during the data collection mode. This instruction is necessary only if an inhibit mask table instruction has been previously executed. The DCM enables the mask table at power-up. Refer to Figure 5-27 for the instruction format and Figure 5-28 for the response format for this instruction.

Figure 5-27 Enable Mask Table Instruction Format

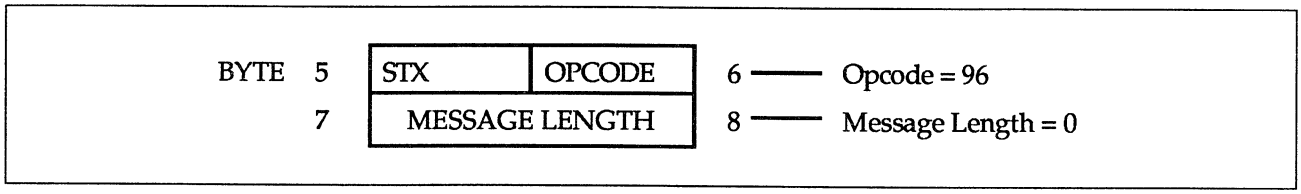
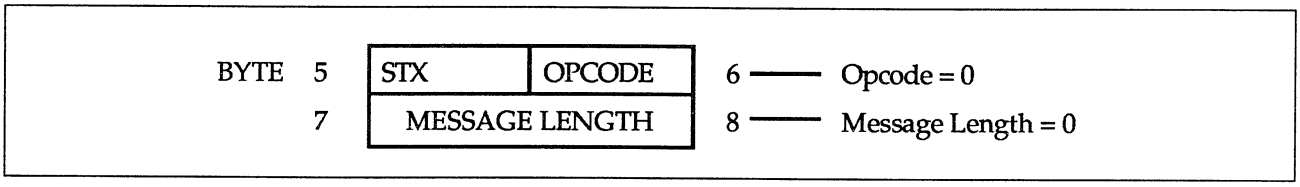


Figure 5-28 Enable Mask Table Response Format (Instruction Executed)



Register Instructions

Purpose

Register instructions:

- obtain or set the contents of individual or groups of locations in the 620 CPM's data registers,
- transfer multiple 16-bit groups of data from I/O modules or the Register Table to the host,
- transfer multiple 16-bit groups of data from the host to I/O modules or to the Register Table, or
- provide access to processor system status information.

Continued on next page

Read N registers, no sign

This instruction reads N contiguous data registers disregarding the sign bit. Refer to Figure 5-29 for the instruction format and Figure 5-30 for the response format for this instruction.

Figure 5-29 Read N Registers (No Sign) Instruction Format

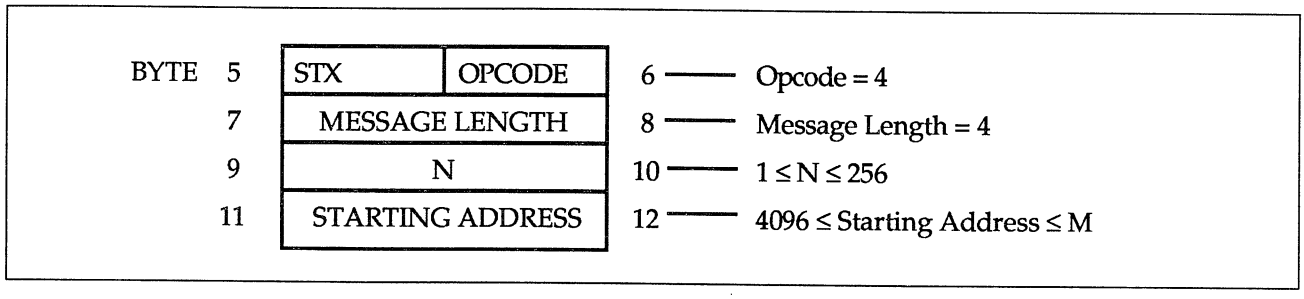
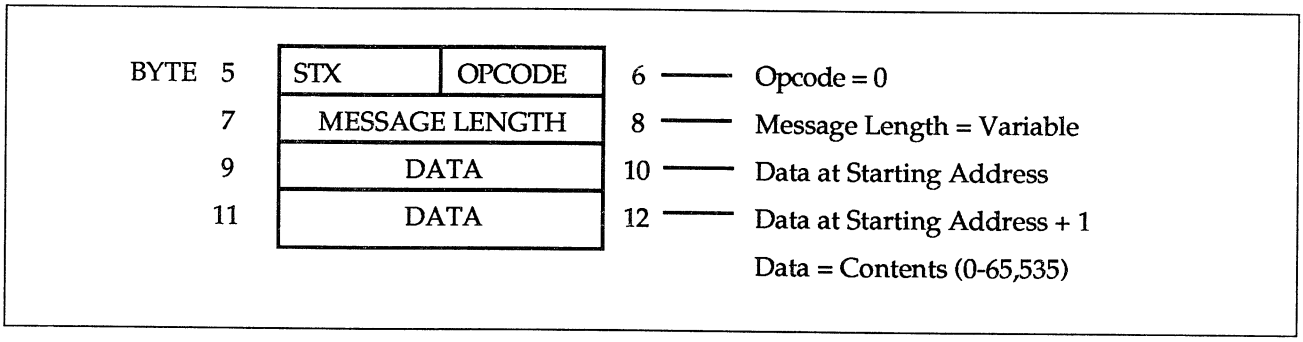


Figure 5-30 Read N Registers (No Sign) Response Format (Instruction Executed)



Continued on next page

Read N signed registers This instruction reads N contiguous signed registers (17 bits total) of the 620-20, 620-25, 620-30, and 620-35 LCSs. In the 620-10, 620-15, 620-12/1633/36, and 620-11/14/1631 LCSs, which do not have signed registers, the sign bit always appears positive. Refer to Figure 5-31 for the instruction format and Figure 5-32 for the response format for this instruction.

Figure 5-31 Read N Signed Registers Instruction Format

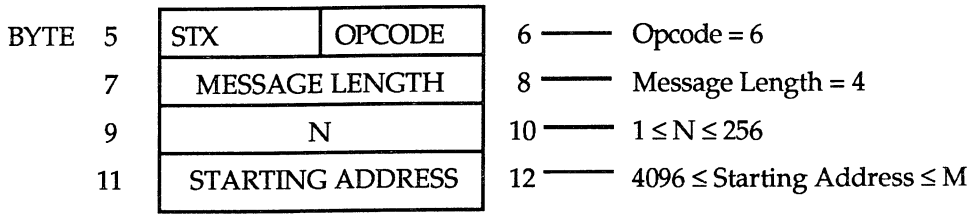
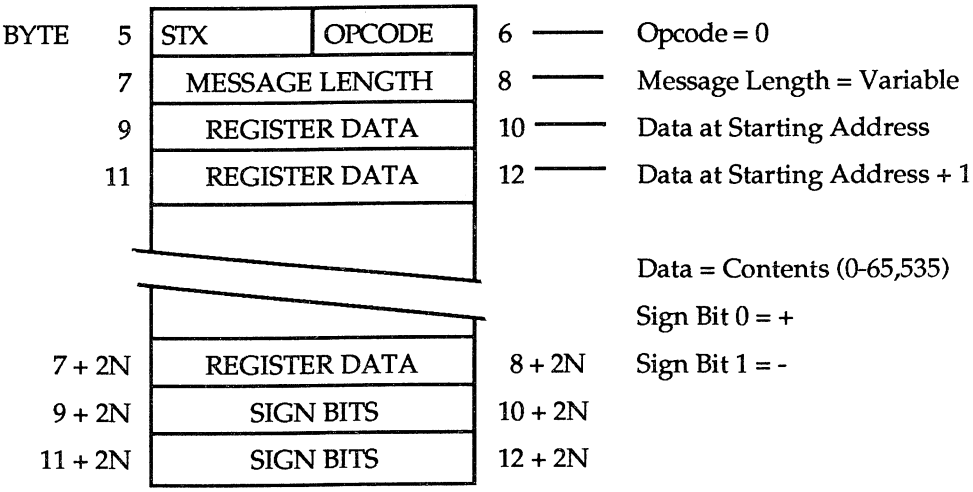


Figure 5-32 Read N Signed Registers Response Format (Instruction Executed)



ATTENTION The sign bits are packed into 16-bit data words following the register data field, with the least significant bit corresponding to the first register's sign-bit status.

Continued on next page

Read N scattered registers

This instruction reads individual registers at various noncontiguous locations in the Data Register Table. The sign bit does not exist in the 620-10, 620-15, 620-12/1633/36, and the 620-11/14/1631 LCSs and is not read when reading scattered registers in the 620-20, 620-25, 620-30, and 620-35 LCSs. Refer to Figure 5-33 for the instruction format and Figure 5-34 for the response format for this instruction.

Figure 5-33 Read N Scattered Registers Instruction Format

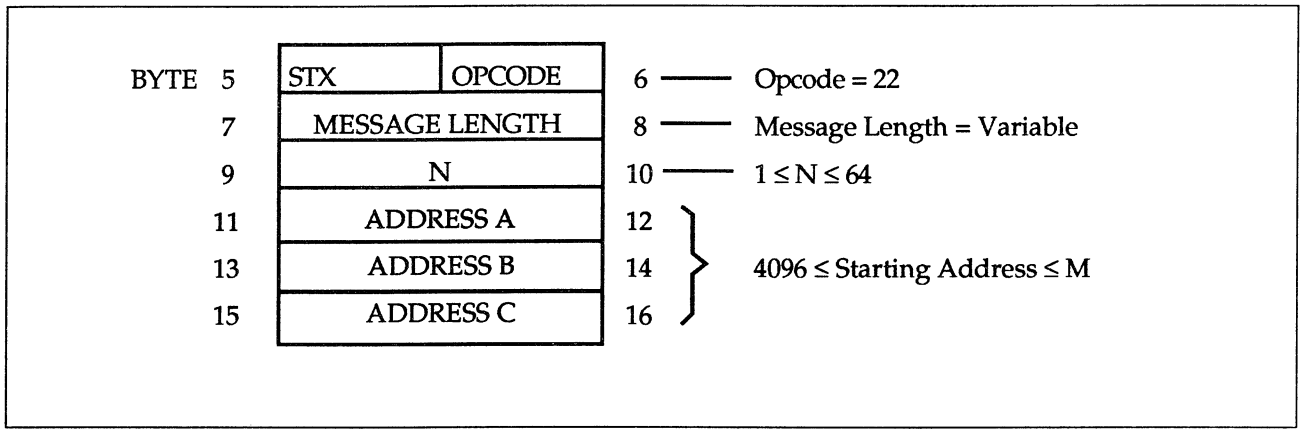
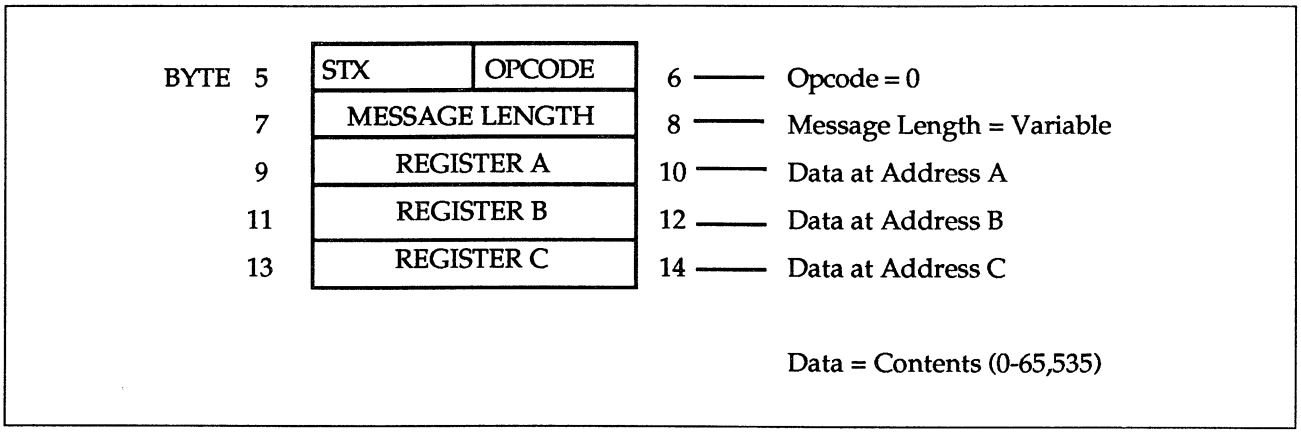


Figure 5-34 Read N Scattered Registers Response Format (Instruction Executed)



Continued on next page

Write N registers, no sign

This instruction writes to individual locations in the Data Register Table and sets the sign bit to positive (+) in LCSs with a 17th bit (that is the 620-20, 620-25, 620-30, and 620-35). The DCM output write protect function must be disabled to execute this instruction. Refer to Figure 5-35 for the instruction format and Figure 5-36 for the repsoinse format for this instruction.

Figure 5-35 Write N Registers (No Sign) Instruction Format

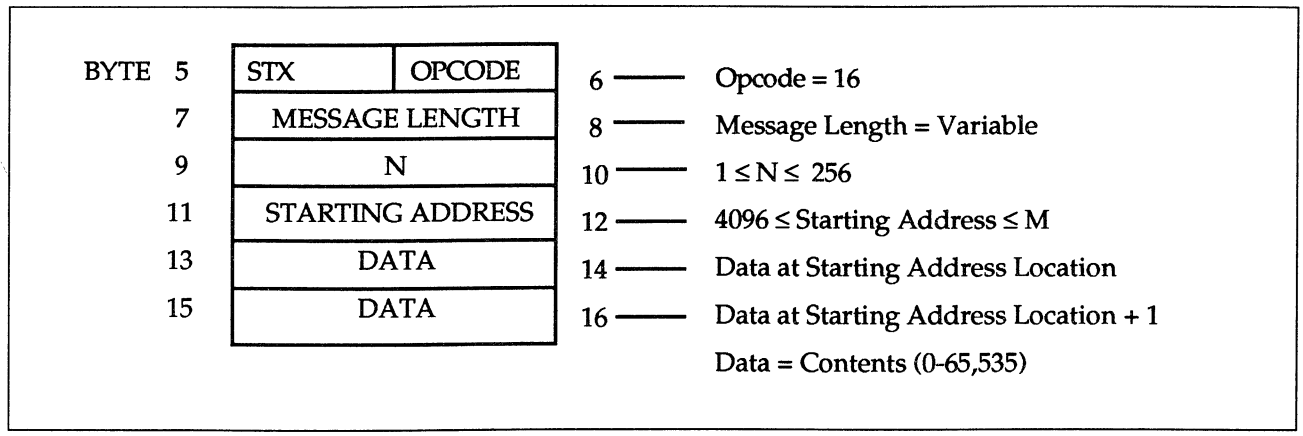
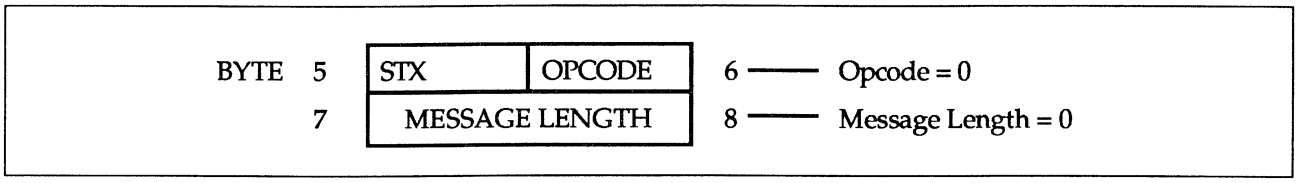


Figure 5-36 Write N Registers (No Sign) Response Format (Instruction Executed)

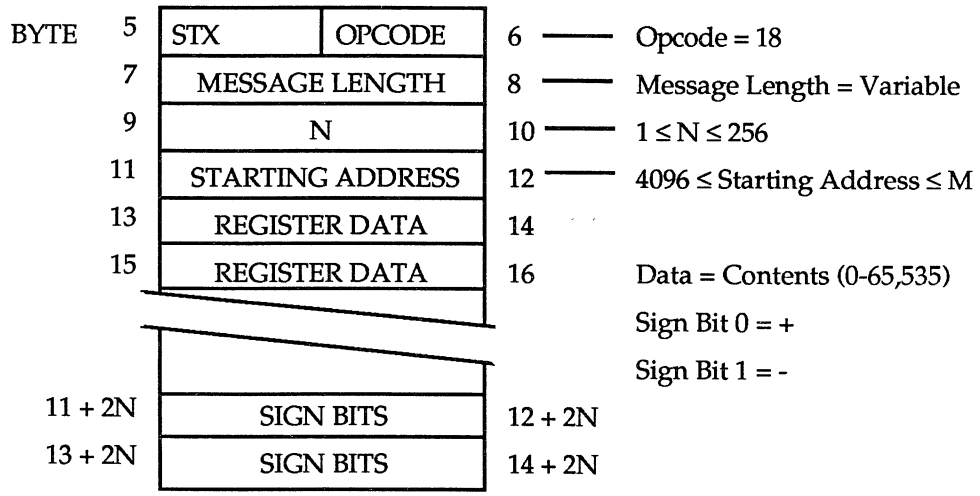


Continued on next page

Write N signed registers

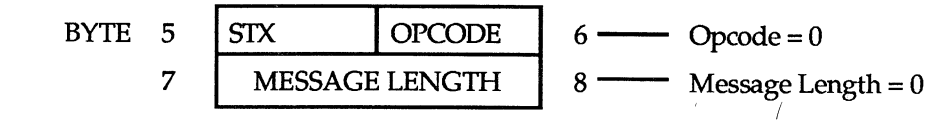
This instruction writes both 16-bit data and sign data (17 bits total) to N contiguous locations in the Data Register Table. The sign bit is dropped in the 620-06/10/15, the 620-11/14/1631, and the 620-12/1633/36 LCSs. The DCM output write protect function must be disabled to execute this instruction. Refer to Figure 5-37 for the instruction format and Figure 5-38 for the response format for this instruction.

Figure 5-37 Write N Signed Registers Instruction Format



ATTENTION The first 16-bit register data word corresponds to the starting address data. The sign bits are packed into 16-bit data words following the register data field, with the least significant bit corresponding to the first register's sign-bit status.

Figure 5-38 Write N Signed Registers Response Format (Instruction Executed)



Continued on next page

Write N scattered registers

This instruction writes to individual registers at various noncontiguous locations in the Data Register Table. Write N Scattered Registers deals only with unsigned 16-bit data and sets the sign bit to positive (+) in processors with a 17th bit (that is, the 620-20, 620-25, 620-30, and 620-35). The DCM output write protect function must be disabled to execute this instruction. Refer to Figure 5-39 for the instruction format and Figure 5-40 for the response format for this instruction.

Figure 5-39 Write N Scattered Registers Instruction Format

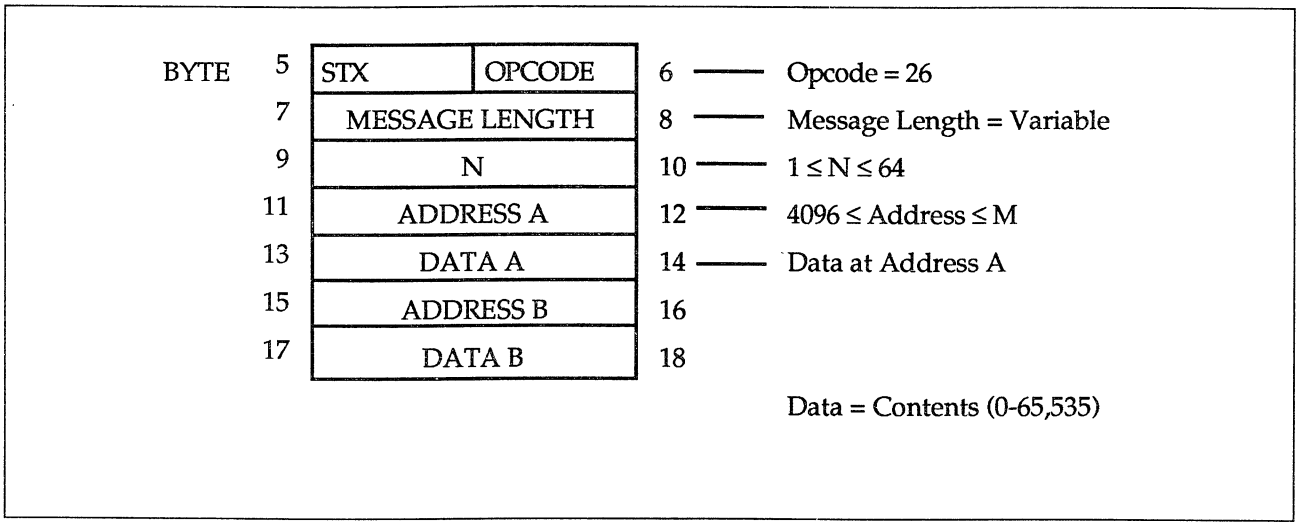
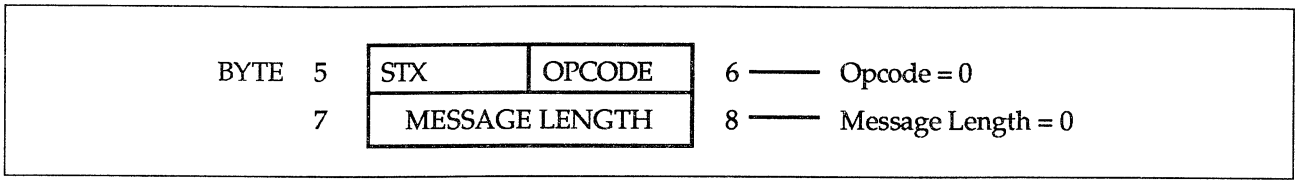


Figure 5-40 Write N Scattered Registers Response Format (Instruction Executed)



Continued on next page

PULL N I/O registers

This instruction is used for fetching N contiguous 16-bit words of data from intelligent I/O modules. The DCM reads data from the I/O module ascending from the starting address. Refer to Figure 5-41 for the instruction format and Figure 5-42 for the response format for this instruction.

ATTENTION This instruction is functional only with the 620 CPM in the RUN, RUN/PROGRAM, or DISABLE mode. The 620-10 does not accept PULL instructions. The PULL instruction can be used only within intelligent I/O modules. Consult the *621 I/O Specifications User Manual* for information on I/O modules that support the PULL instruction.

Figure 5-41 PULL N I/O Registers Instruction Format

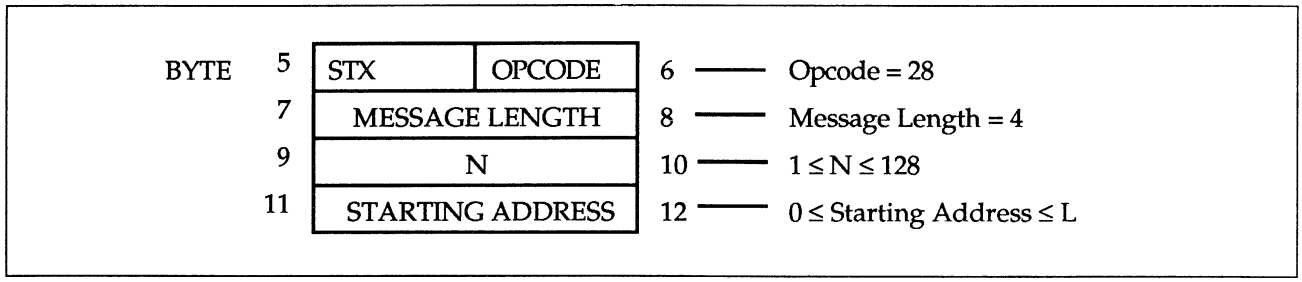
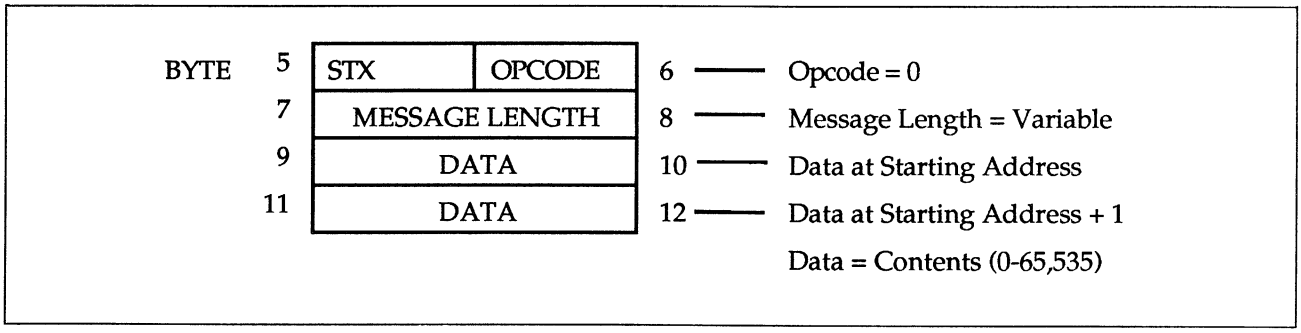


Figure 5-42 PULL N I/O Registers Response Format (Instruction Executed)



Continued on next page

PUSH N I/O registers

This instruction writes 16-bit words to intellignet I/O modules. The DCM writes data to the I/O module ascending from the starting address. Refer to Figure 5-43 for the instruction format and Figure 5-44 for the response format for this instruction.

ATTENTION This instruction is functional only with the 620 CPM in the RUN or RUN/PROGRAM mode. The 620-10 does not accept PUSH instructions. The DCM output write protect function must be disabled to execute this instruction. The PUSH instructions can be used only with intelligent I/O modules. Consult the *621 I/O Specifications User Manual* for more information on I/O modules that support the PUSH instruction.

Figure 5-43 PUSH N I/O Registers Instruction Format

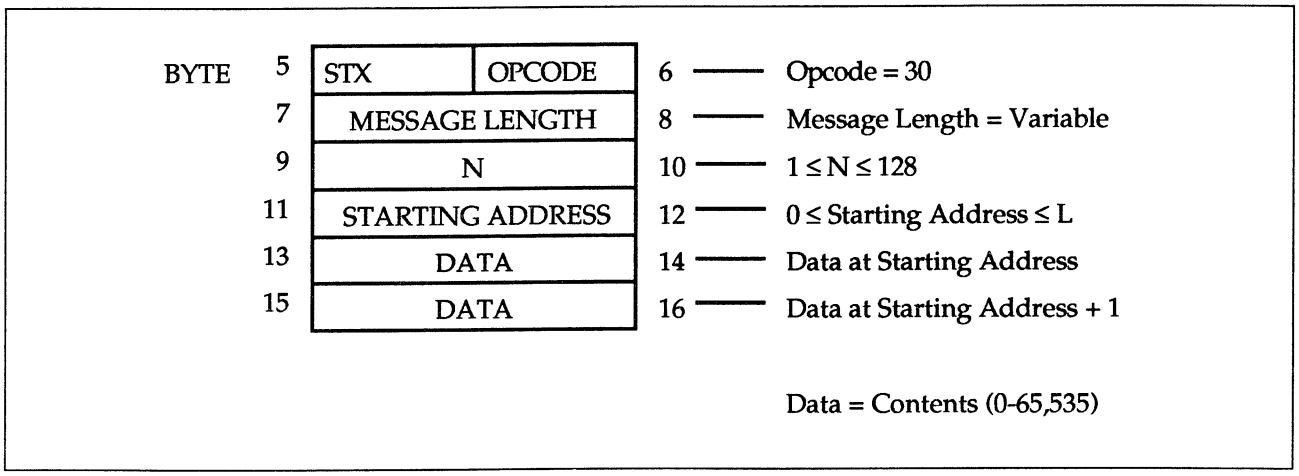
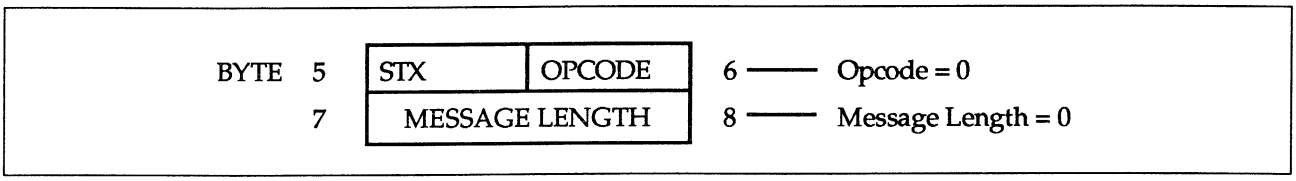


Figure 5-44 PUSH N I/O Registers Response Format (Instruction Executed)



Continued on next page

Read N system status registers

This instruction gathers system identification, status, and diagnostic information from the 620 CPM. The registers are read in pairs to satisfy the word format and are read from the most significant address of the desired memory block. The 8-bit registers are read into 16-bit words downwards from the starting address. Refer to Figure 5-45 for the instruction format and Figure 5-46 for the response format for this instruction.

Figure 5-45 Read N System Status Registers Instruction Format

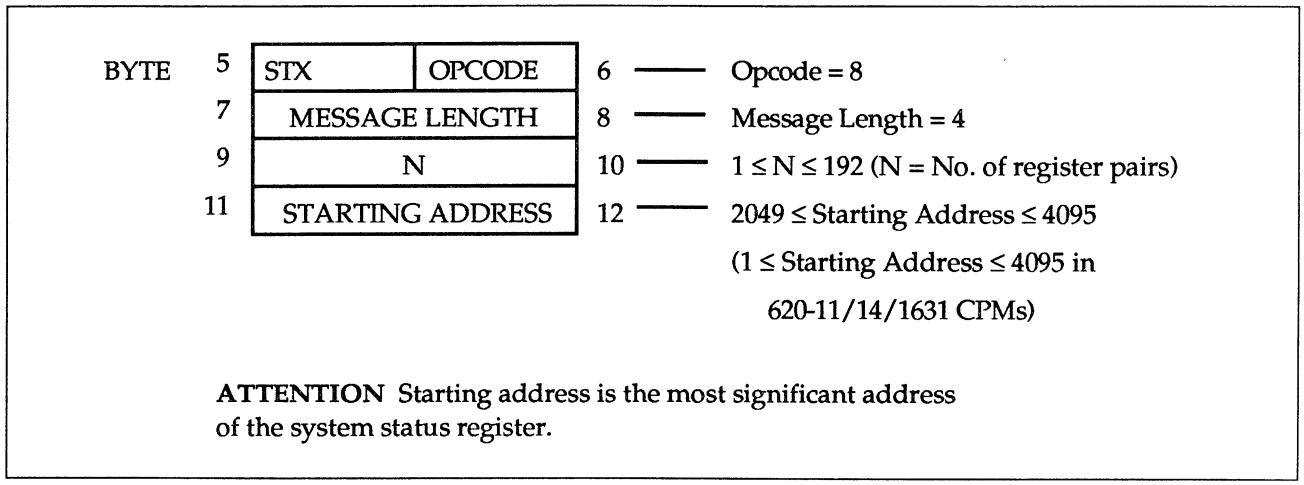
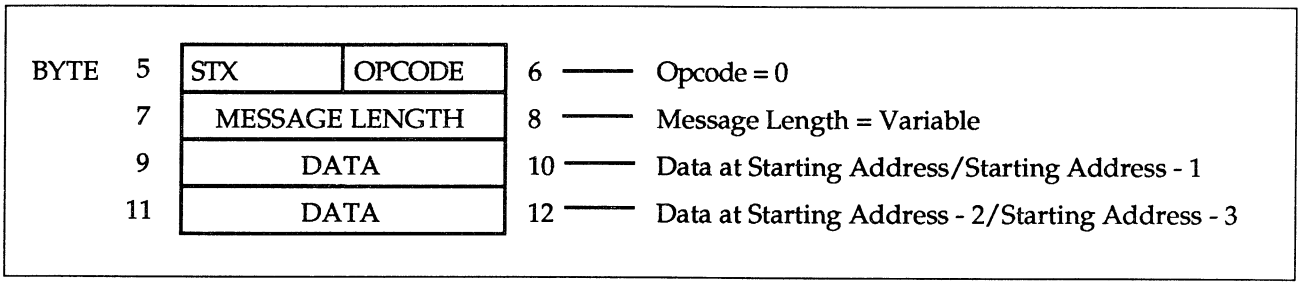


Figure 5-46 Read N System Status Registers Response Format (Instruction Executed)



Continued on next page

Write N system status registers

This instruction allows you to write N contiguous 8-bit System Status Table registers starting at the specified address and working downward. The command can be executed in any 620 CPM mode. The memory write protect function must be disabled. Refer to Figure 5-47 for the instruction format and Figure 5-48 for the response format for this instruction.

Figure 5-47 Write N System Status Registers Instruction Format

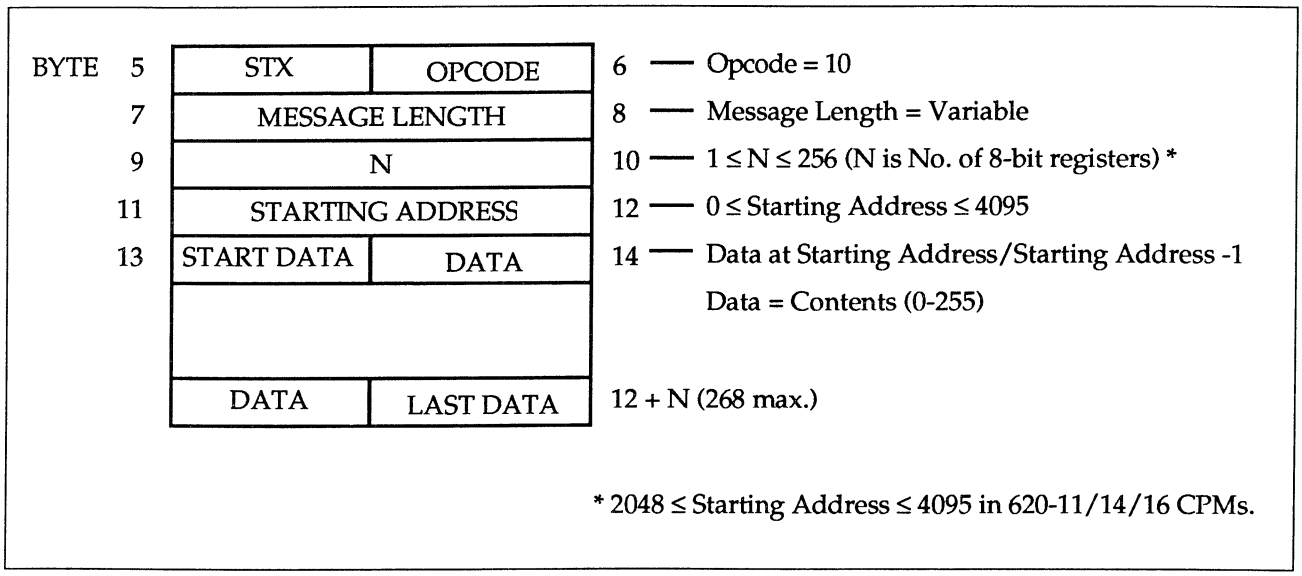
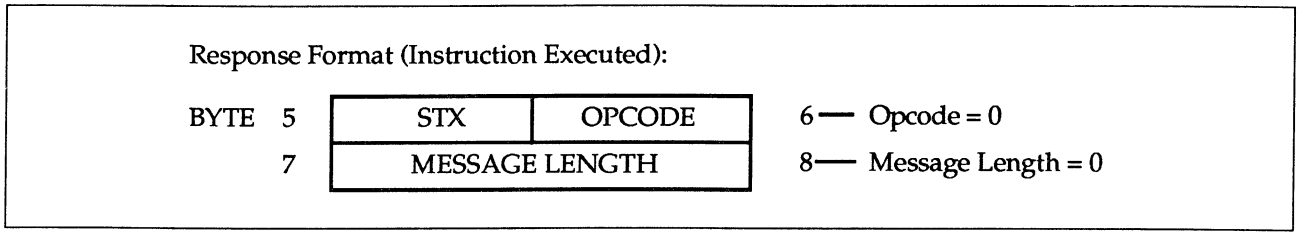


Figure 5-48 Write N System Status Registers Response Format (Instruction Executed)



WARNING

WARNING: Misuse may halt the 620 CPM. Refer to the specific 620 LCS user manual for more information regarding writing to the System Status Table.

620 LCS Processor Control Instructions

Purpose

620 LCS processor control instructions either place the 620 CPM into or remove it from the PROGRAM mode. These instructions are used with instructions that require such a processor mode change.

Continued on next page

Request PROGRAM mode

This instruction requests PROGRAM mode control for the DCM. Refer to Figure 5-49 for the instruction format and Figure 5-50 for the response format for this instruction.

ATTENTION This request must be granted by the 620 CPM before the DCM accepts program memory instructions. When multiple requests are pending, the 620 CPM grants them in order of rank. The 623 Loader/Terminal is given highest priority and option modules follow in order from lowest to highest card address. Once a request is submitted, it must be removed by the host computer when it is no longer needed. Refer to the specific 620 LCS user manual for more information regarding writing to the System Status Table.

Figure 5-49 Request PROGRAM Mode Instruction Format

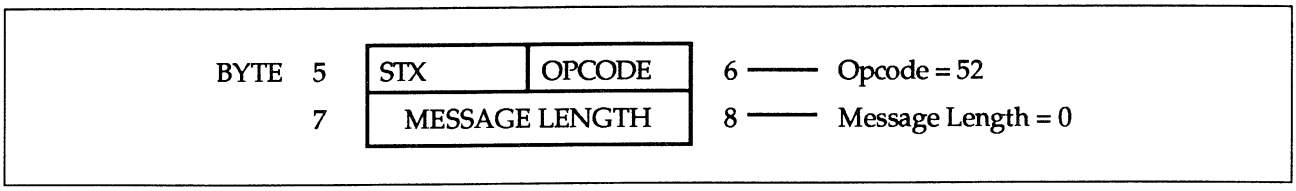
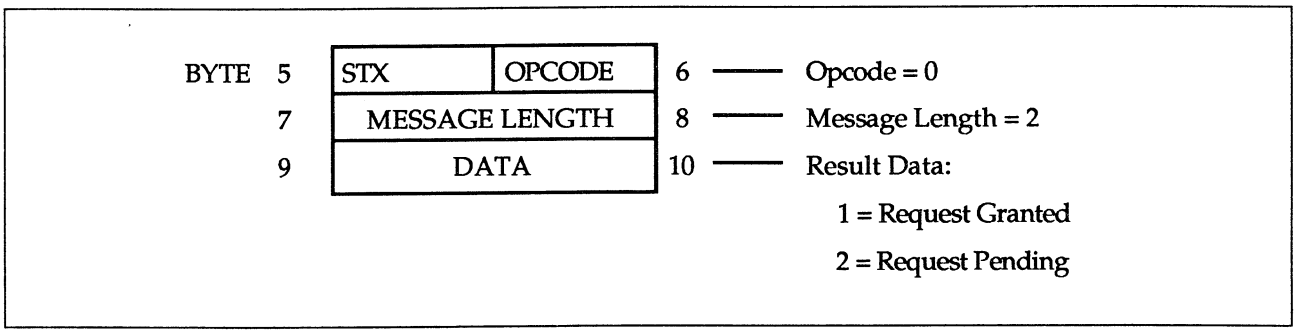


Figure 5-50 Request PROGRAM Mode Response Format (Instruction Executed)



Continued on next page

Remove PROGRAM mode request

This instruction removes the software PROGRAM mode request. If no other PROGRAM mode requests are pending, the 620 CPM returns to the mode specified by the processor keyswitch. Refer to Figure 5-51 for the instruction format and Figure 5-52 for the response format for this instruction.

Figure 5-51 Remove PROGRAM Mode Request Instruction Format

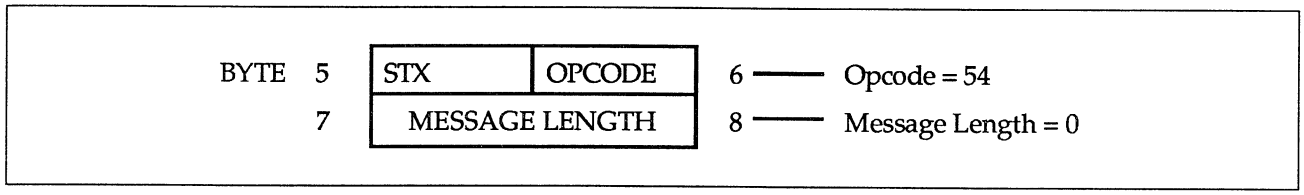
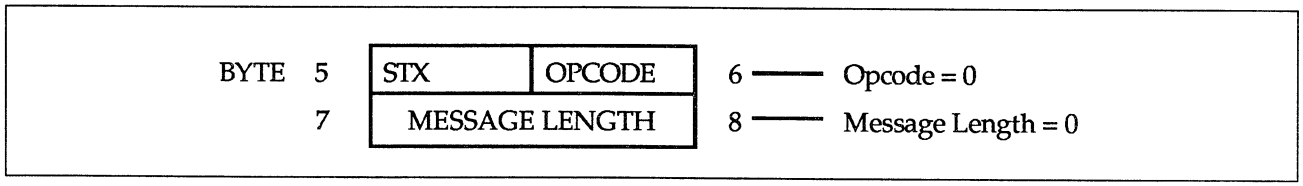


Figure 5-52 Remove PROGRAM Mode Request Response Format (Instruction Executed)



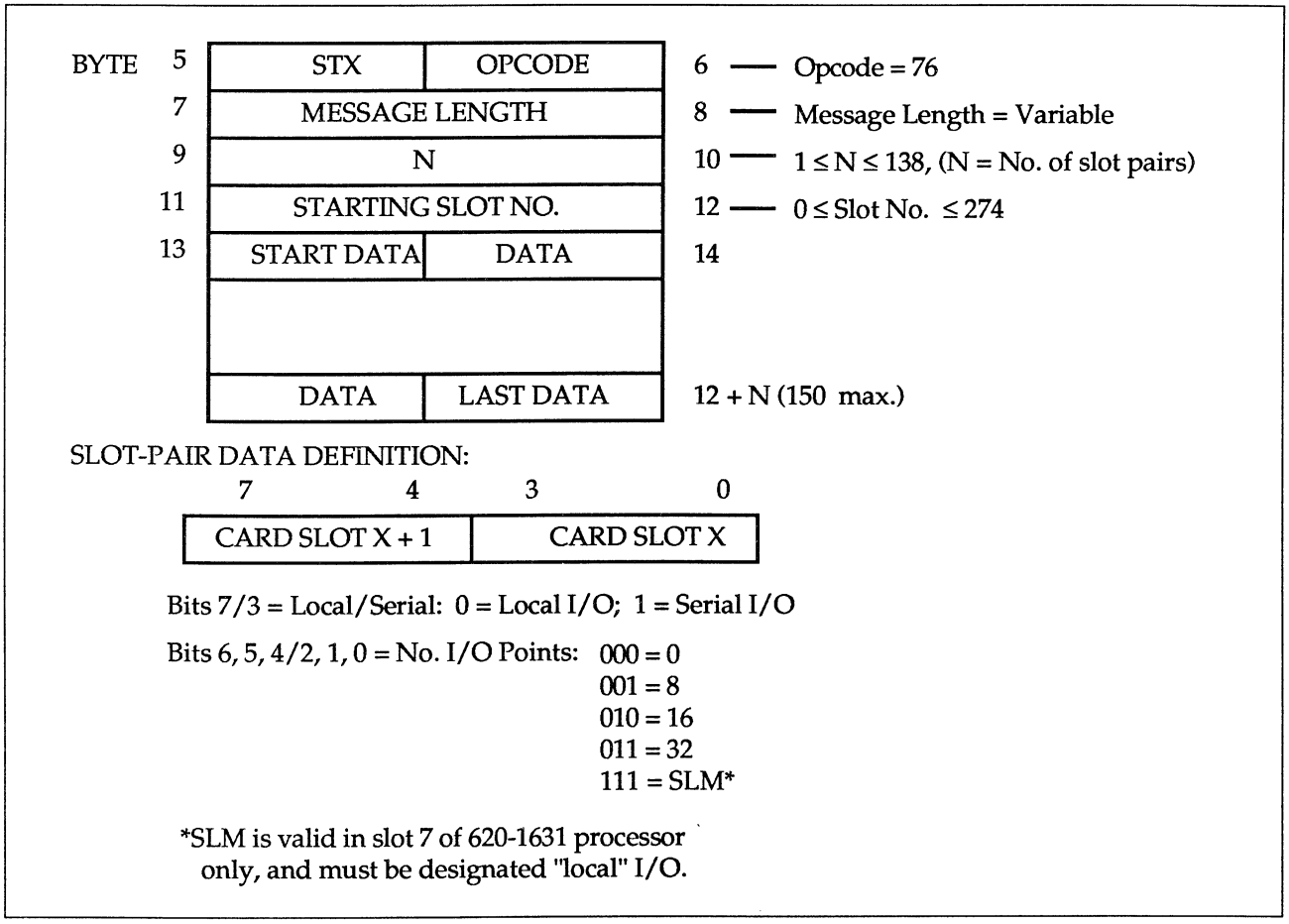
Continued on next page

Write I/O configuration

This instruction allows you to configure the I/O module slots in the 620-11/14/1631 LCSs for 0-, 8-, 16-, or 32-point operation and for local or serial operation. The command writes N contiguous bytes of packed slot configuration data (2 slots/byte) to the System Status Table starting at the specified slot number aned working upward. Refer to Figure 5-53 for the instruction format and Figure 5-54 for the response format for this instruction.

ATTENTION The starting slot number must be an even number. The command will be executed in any 620 CPM mode. The memory write protect function must be disabled.

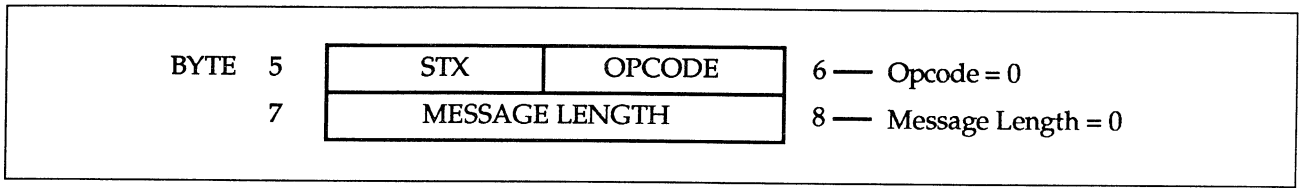
Figure 5-53 Write I/O Configuration Instruction Format



Continued on next page

Write I/O configuration,
continued

Figure 5-54 Write I/O Configuration Response Format (Instruction Executed)



ATTENTION

ATTENTION: Refer to the specific 620 LCS user manual for more information regarding writing the I/O configurations.

Continued on next page

Write processor control configuration

This instruction allows you to configure the I/O and mode control functions for the 620-12/1633/36 LCSs. The instruction will be executed in any CPM mode. The memory write protect function must be disabled. Refer to Figure 5-55 for the instruction format and Figure 5-56 for the response format for this instruction.

Figure 5-55 Write Processor Control Configuration Instruction Format

BYTE			
5	STX	OPCODE	6 — Opcode = 78
7	MESSAGE LENGTH		8 — Message Length = 2
9	DATA 2	DATA 1	10

DATA 1

PROCESSOR CONTROL DATA DEFINITION:

7	6	5	4	3	2	1	0
		Scan Loss	Data Chng	Low Batt	Out Stat	Force	ARMP

Bits 7, 6 = Not Used: 00
Bit 5 = Scan Loss Timer: 0 = disabled; 1 = enabled
Bit 4 = Data Change Function: 0 = disabled; 1 = enabled
Bit 3 = Scan with Low Battery: 0 = disabled; 1 = enabled
Bit 2 = Output Status in Program/Disable Modes: 0 = freeze; 1 = clear
Bit 1 = Force Function: 0 = disabled; 1 = enabled
Bit 0 = Augmented Run Mode Programming: 0 = disabled; 1 = enabled

DATA 2

PROCESSOR CONTROL DATA DEFINITION:

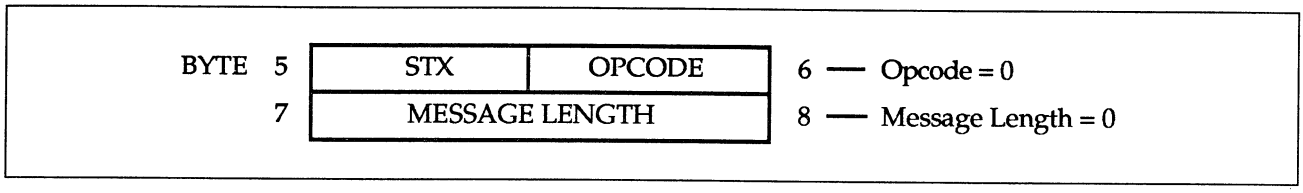
7	6	5	4	3	2	1	0
Multi-drop enable			Nodal Addr	Nodal Addr	Nodal Addr	Nodal Addr	Nodal Addr

Bit 7 = Multidrop Loader Port Enable:
0 = point-to-point; 1 = Multidrop
Bits 6, 5 = Not used: 00
Bits 4, 3, 2, 1, 0 = Loader Port Nodal Address

Continued on next page

Write processor control configuration, continued

Figure 5-56 Write Processor Control Configuration Response Format (Instruction Executed)



ATTENTION

ATTENTION: Refer to the specific 620 LCS user manual for more information regarding writing the I/O configurations.

Program Memory Instructions

Purpose

Program memory instructions manipulate program memory.

Continued on next page

Upload N program memory words

This instruction uploads program memory. The instruction fetches up to 150 of the 24-bit memory words and packs each into two 16-bit data words. This instruction is executed with the 620 CPM in any mode. Refer to Figure 5-57 for the instruction format and Figure 5-58 for the response format for this instruction.

Figure 5-57 Upload N Program Memory Words Instruction Format

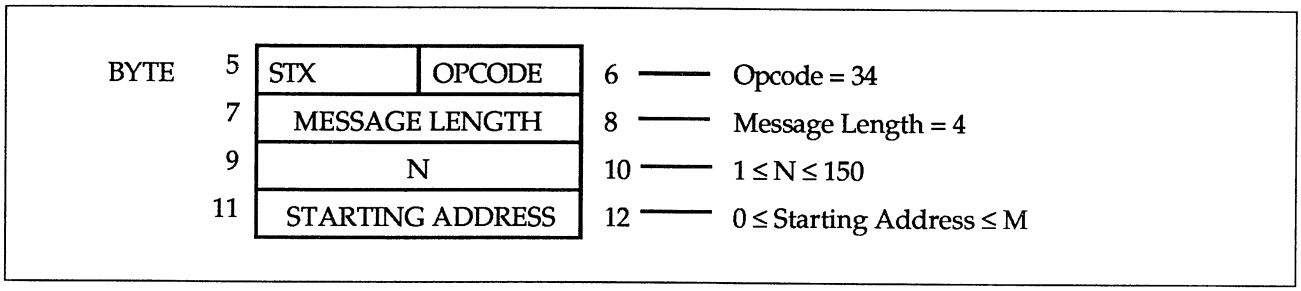
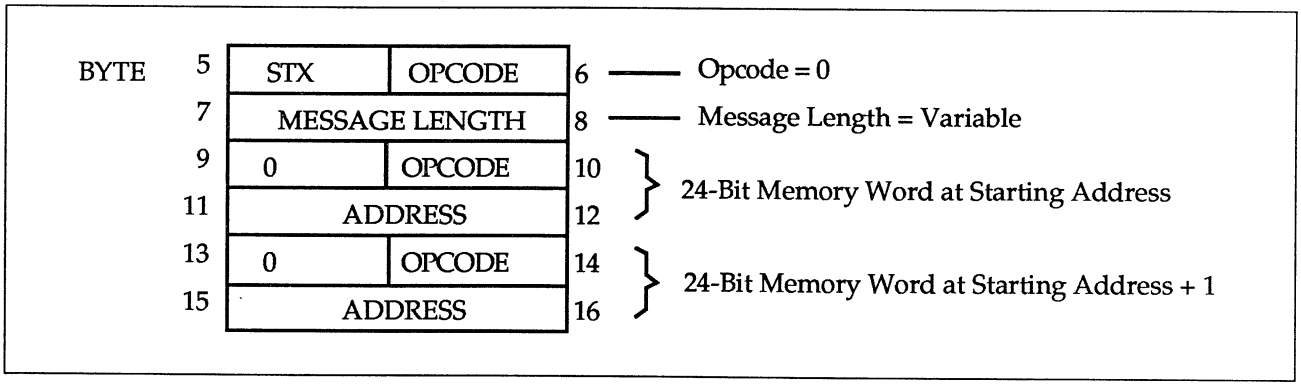


Figure 5-58 Upload N Program Memory Words Response Format (Instruction Executed)



Continued on next page

Download N Program Memory Words

This instruction downloads program memory. The instruction writes up to 150 of the 24-bit words, extracted from two packed 16-bit data words. It is executed with the 620 CPM keyswitch in any position. Refer to Figure 5-59 for the instruction format and Figure 5-60 for the response format for this instruction.

ATTENTION

- When the 620 CPM is in the RUN mode, this instruction can be executed without a software PROGRAM mode request. The processor force count is adjusted if forced opcodes are downloaded or overwritten and End of Memory (EOM) is not altered.
- When the 620 CPM is in the PROGRAM mode, this instruction is accepted only while the DCM has the processor in the software PROGRAM mode. This is necessary to eliminate contention between multiple user memory programmers.
- The DCM program memory write protect function must be disabled to execute this instruction.

Figure 5-59 Download N Program Memory Words Instruction Format

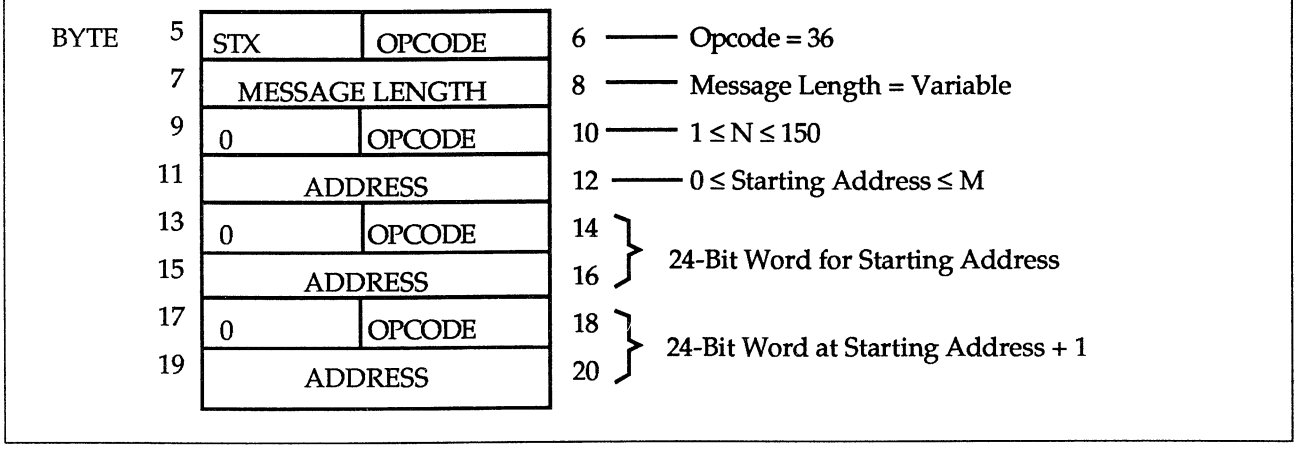
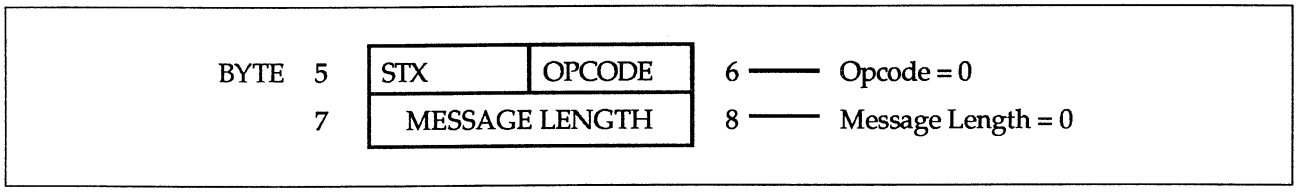


Figure 5-60 Download N Program Memory Words Response Format (Instruction Executed)



Continued on next page

Clear program memory

This instruction effectively erases the program memory I/O Status Tables, register tables, force count, and fault count. Refer to Figure 5-61 for the instruction format and Figure 5-62 for the response format for this instruction.

ATTENTION This instruction is accepted only while the DCM has the processor in the software PROGRAM mode and the DCM program memory write protect function is disabled.

Figure 5-61 Clear Program Memory Instruction Format

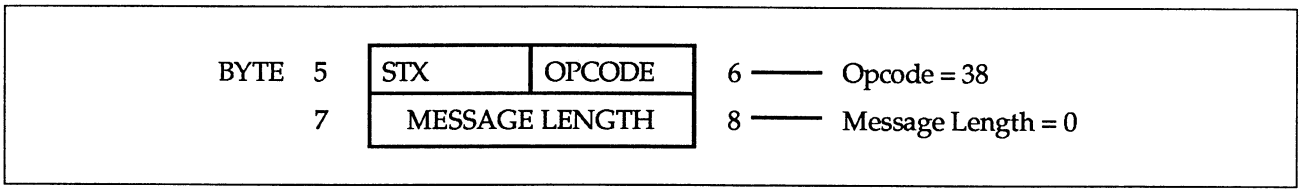
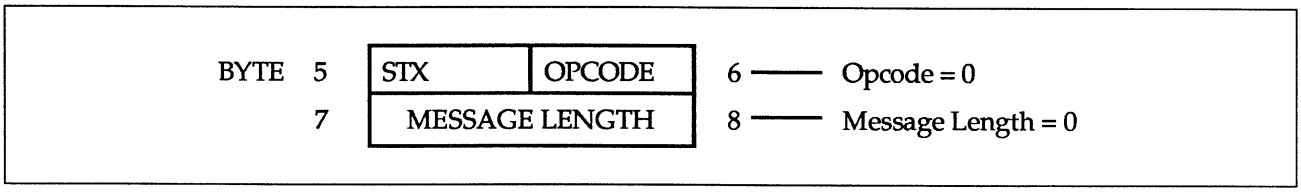


Figure 5-62 Clear Program Memory Response Format (Instruction Executed)



Continued on next page

Insert N program memory words

This instruction is used for editing existing program memory or writing a new program. The instruction inserts up to 150 of the 24-bit memory words by first shifting up the program memory N memory words then writing in the received words. The starting address points to the first word shifted up, therefore the insertion occurs in front of the starting address. If the processor memory is cleared, the insertion occurs before the End of Memory (EOM) opcode, therefore it is not necessary to insert the EOM opcode. Refer to Figure 5-63 for the instruction format and Figure 5-64 for the response format for this instruction.

ATTENTION This instruction is accepted only while the DCM has the 620 CPM in the software PROGRAM mode. The processor force count is adjusted if forced opcodes are inserted and the EOM is not inserted. The DCM program memory write protect function must be disabled.

Figure 5-63 Insert N Program Memory Words Instruction Format

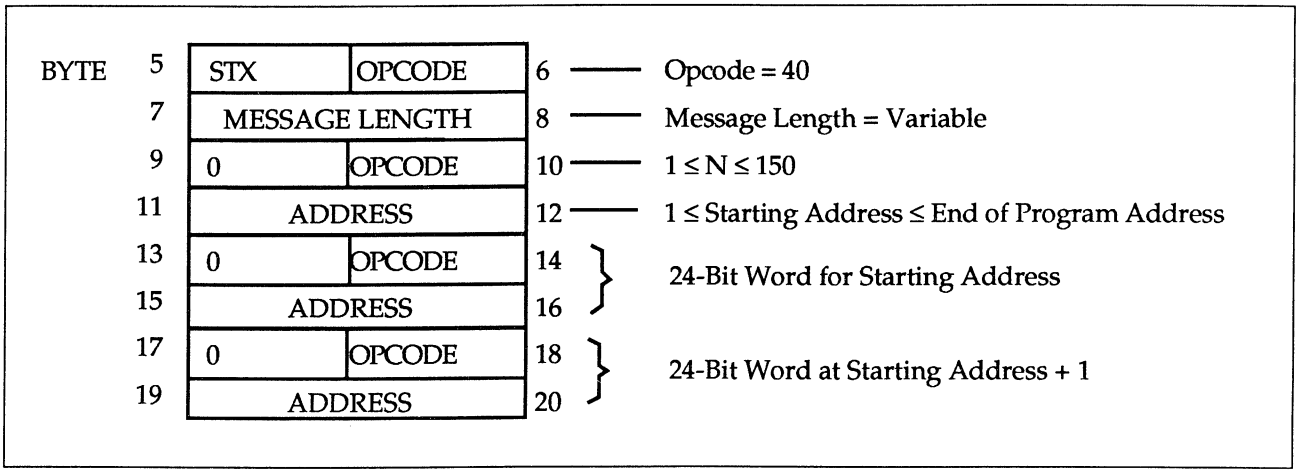
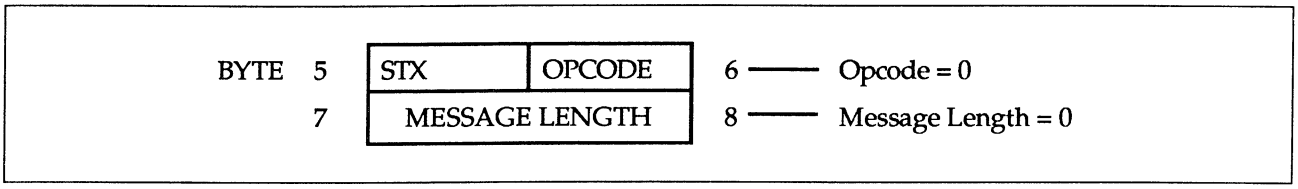


Figure 5-64 Insert N Program Memory Words Response Format (Instruction Executed)



Continued on next page

Delete N program memory words

This instruction edits the program memory. The instruction deletes up to the full program memory, starting with the word pointed to by the starting address. Any program memory remaining above the deleted block is then shifted to join any memory below the starting address. The force count is updated accordingly. Refer to Figure 5-65 for the instruction format and Figure 5-66 for the response format for this instruction.

ATTENTION This instruction is accepted only while the DCM has the 620 CPM in the software PROGRAM mode. The DCM program memory write protect function must be disabled to execute this function.

Figure 5-65 Delete N Program Memory Words Instruction Format

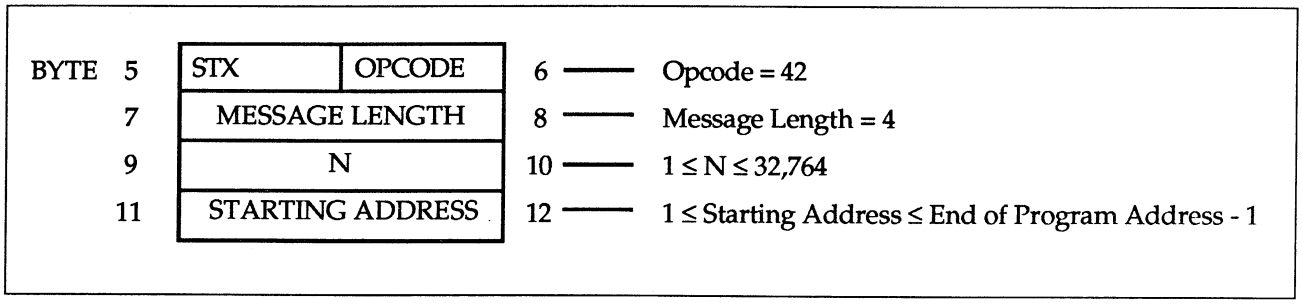
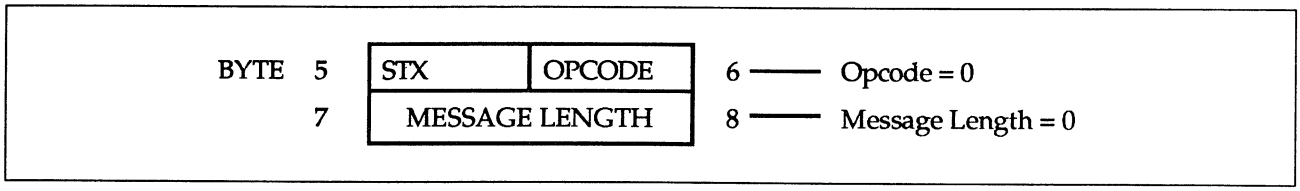


Figure 5-66 Delete N Program Memory Words Response Format (Instruction Executed)



Program Header Instructions

Purpose

Program header instructions upload and download program header information. These instructions must be encoded in ASCII (refer to Table A-2 in the *Appendix* for ASCII-to-decimal conversions).

Continued on next page

Upload program date

This instruction uploads the program date information from registers in the System Status Table. Refer to Figure 5-67 for the instruction format and Figure 5-68 for the response format for this instruction.

ATTENTION This instruction is executed with the 620 CPM in any mode.

Figure 5-67 Upload Program Date Instruction Format

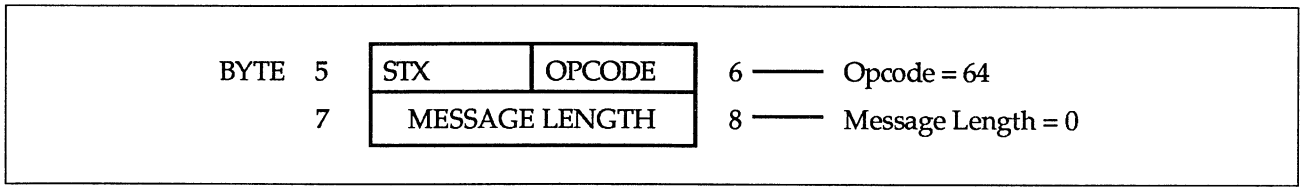
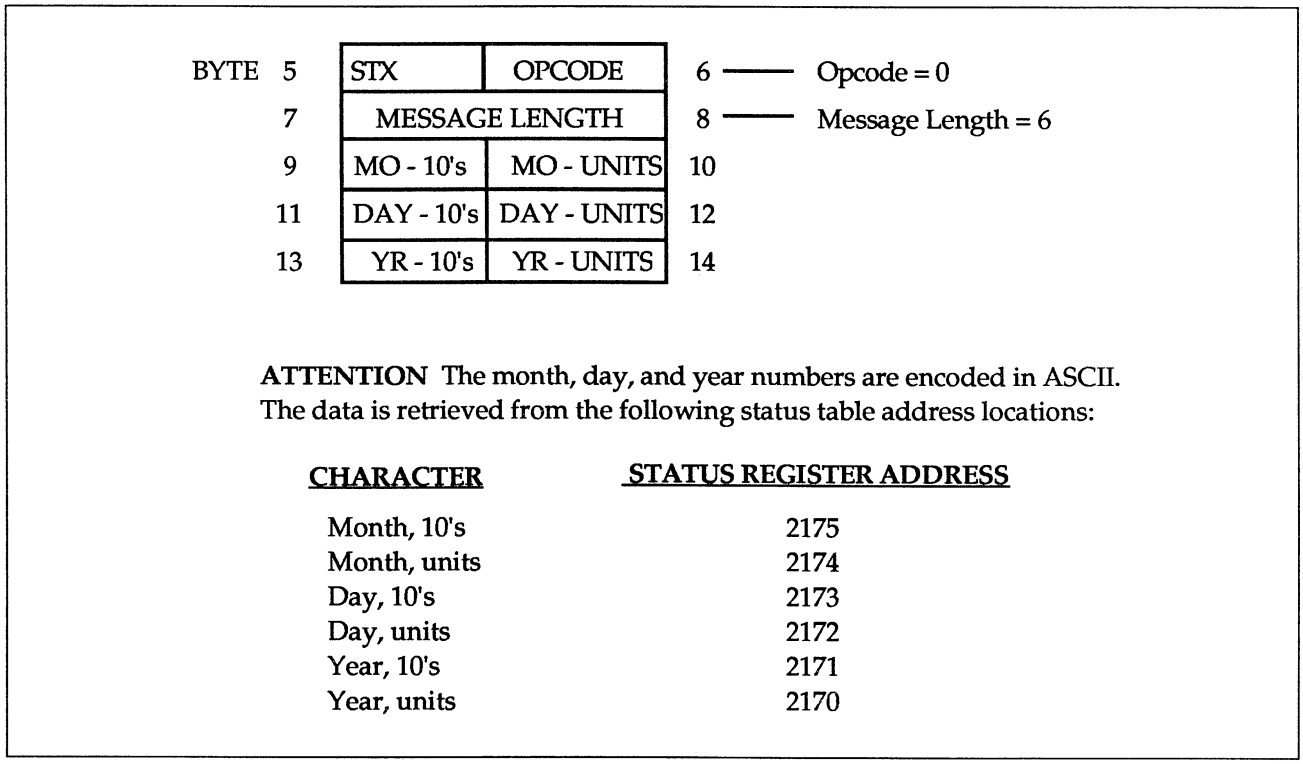


Figure 5-68 Upload Program Date Response Format (Instruction Executed)



ATTENTION The month, day, and year numbers are encoded in ASCII. The data is retrieved from the following status table address locations:

CHARACTER	STATUS REGISTER ADDRESS
Month, 10's	2175
Month, units	2174
Day, 10's	2173
Day, units	2172
Year, 10's	2171
Year, units	2170

Continued on next page

Upload programmer

This instruction reads the programmer information registers in the System Status Table. Refer to Figure 5-69 for the instruction format and Figure 5-70 for the response format for this instruction.

ATTENTION This instruction is executed with the 620 CPM in any mode.

Figure 5-69 Upload Programmer Instruction Format

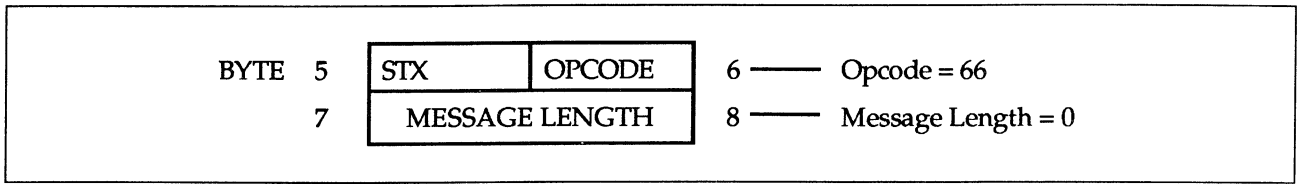
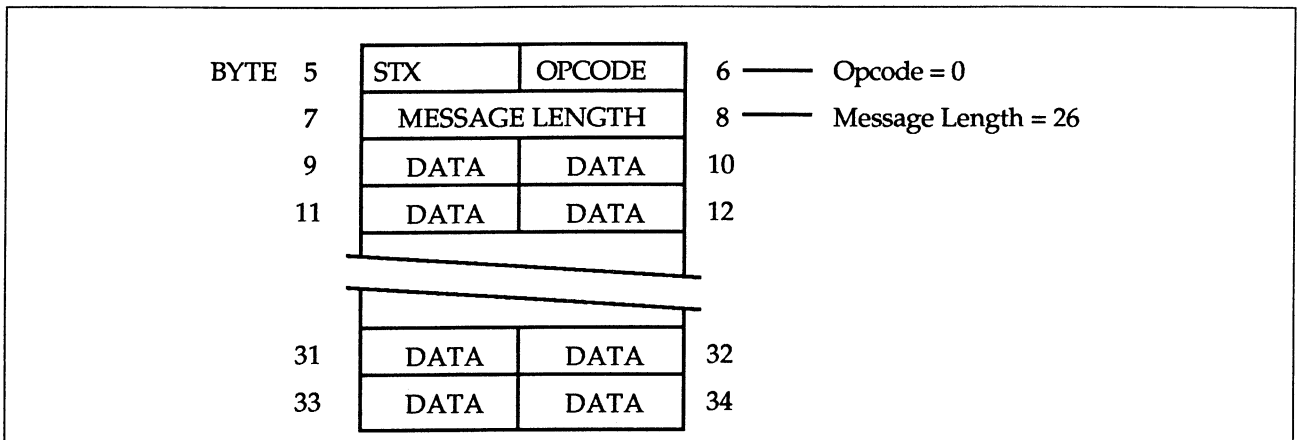


Figure 5-70 Upload Programmer Response Format (Instruction Executed)



ATTENTION Data is encoded in ASCII. It is retrieved from the System Status Table from address 2169 (byte 9) to 2144 (byte 34). Byte 9 contains the first byte of programmer information.

Continued on next page

Upload title

This instruction reads the program title information from system status registers. The instruction is executed with the 620 CPM in any mode. Refer to Figure 5-71 for the instruction format and Figure 5-72 for the response format.

Figure 5-71 Upload Title Instruction Format

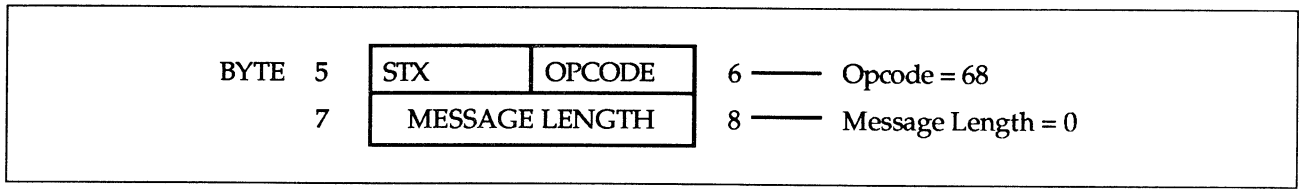
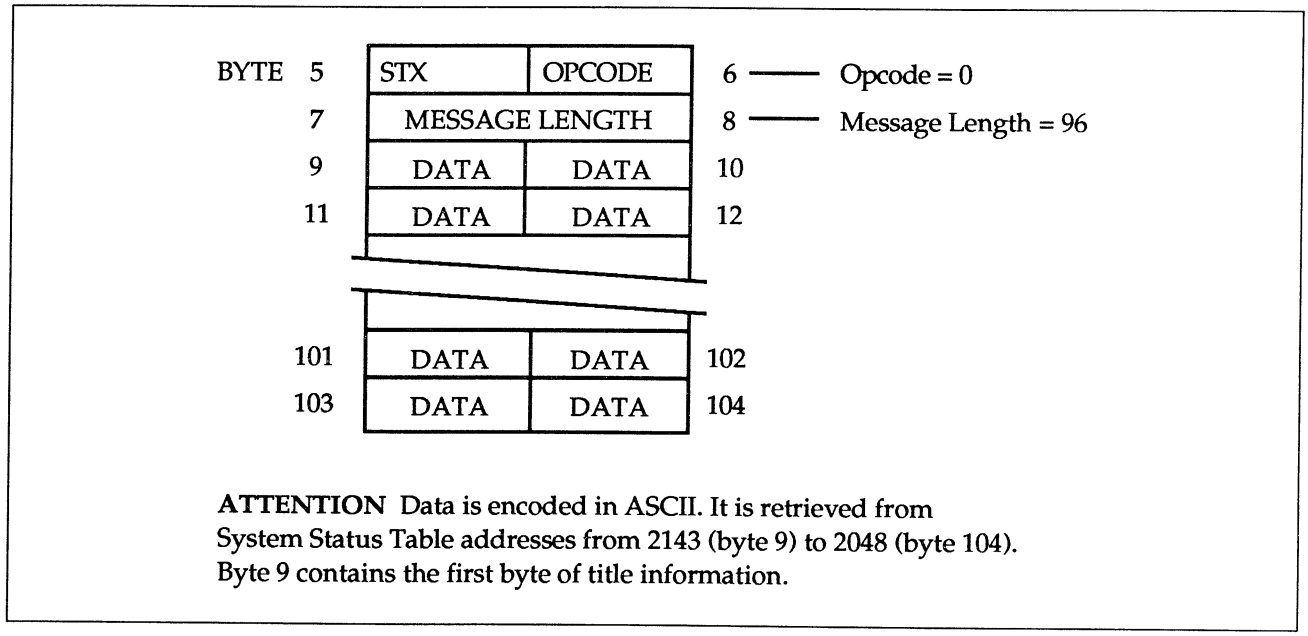


Figure 5-72 Upload Title Response Format (Instruction Executed)



ATTENTION Data is encoded in ASCII. It is retrieved from System Status Table addresses from 2143 (byte 9) to 2048 (byte 104). Byte 9 contains the first byte of title information.

Continued on next page

Download program date

This instruction writes program date information into System Status Table registers. Refer to Figure 5-73 for the instruction format and Figure 5-74 for the response format.

ATTENTION The instruction is executed only while the DCM has the 620 CPM in the software PROGRAM mode. The DCM program memory write protect function must be disabled to execute this instruction.

Figure 5-73 Download Program Date Instruction Format

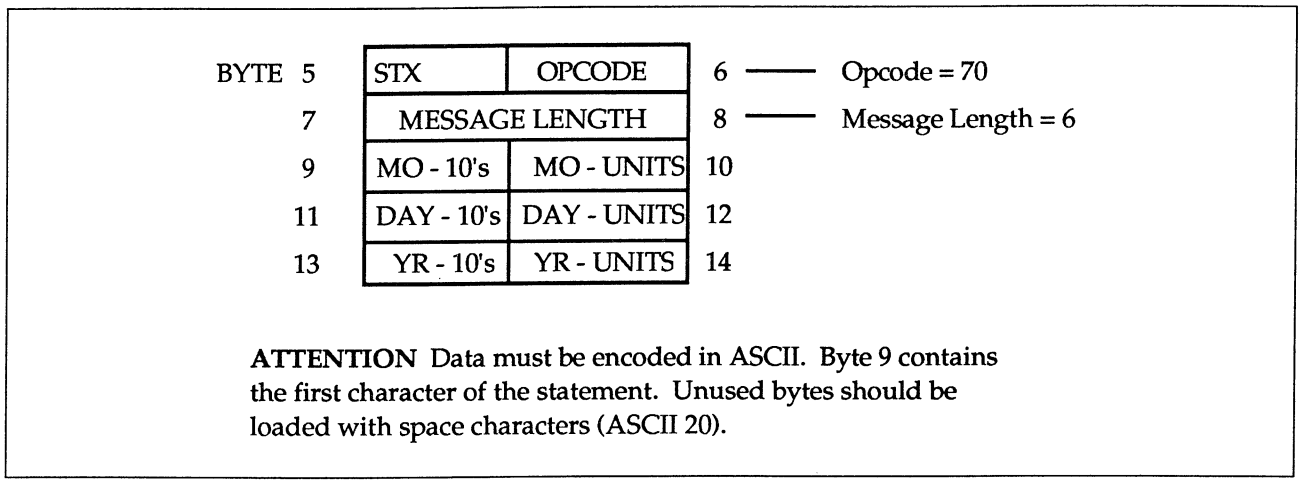
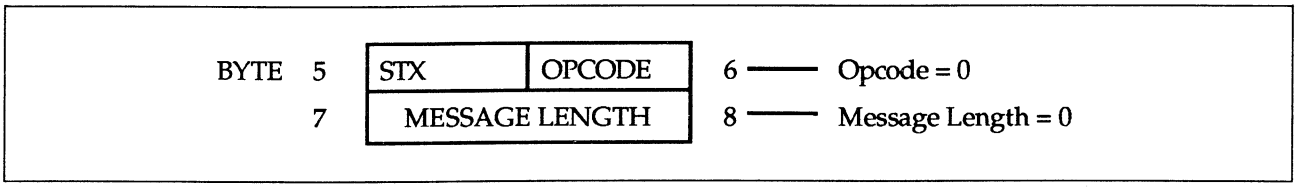


Figure 5-74 Download Program Date Response Format (Instruction Executed)



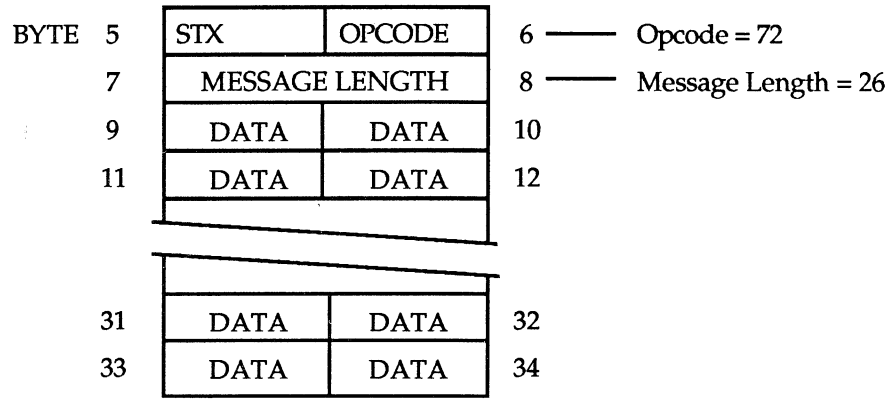
Continued on next page

Download programmer

This instruction writes programmer information into System Status Table registers. Refer to Figure 5-75 for the instruction format and Figure 5-76 for the response format for this instruction.

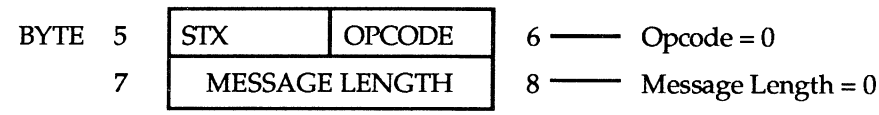
ATTENTION This instruction is executed only when the DCM has placed the 620 CPM in the software PROGRAM mode. The DCM program memory write protect function must be disabled to execute this instruction.

Figure 5-75 Download Programmer Instruction Format



ATTENTION Data must be encoded in ASCII. Byte 9 contains the first character of the statement. Unused bytes should be filled with space characters (ASCII 20).

Figure 5-76 Download Programmer Response Format (Instruction Executed)



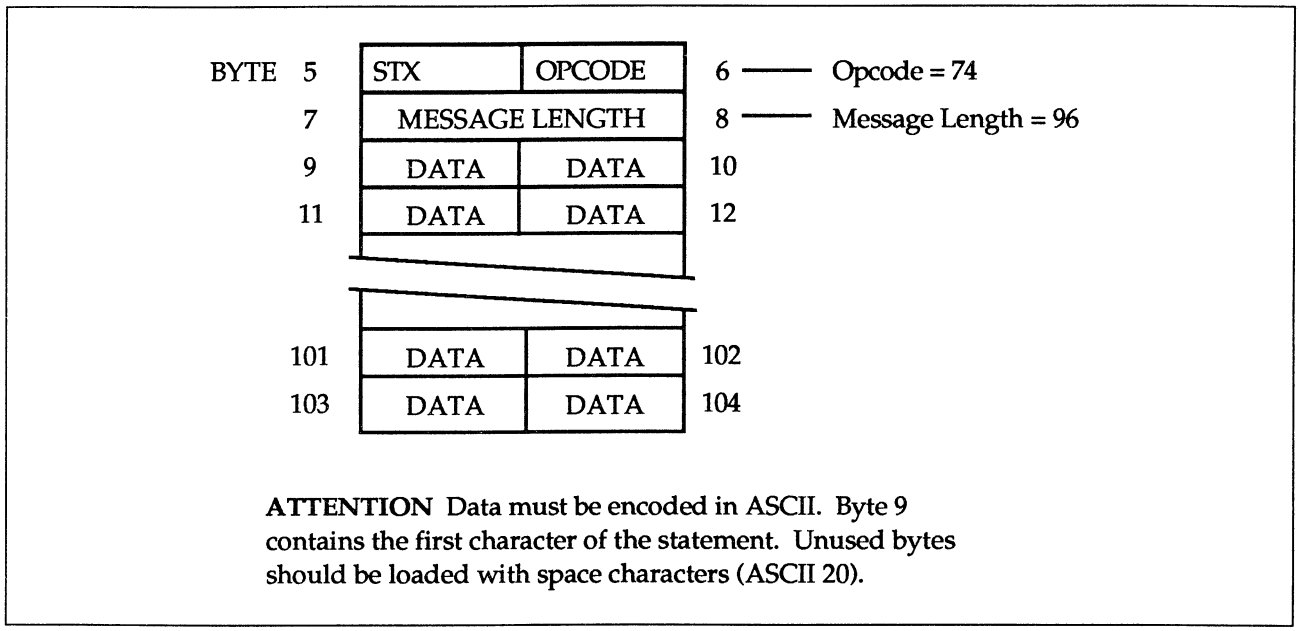
Continued on next page

Download title

This instruction downloads program title information in the System Status Table registers. Refer to Figure 5-77 for the instruction format and Figure 5-78 for the response format for this instruction.

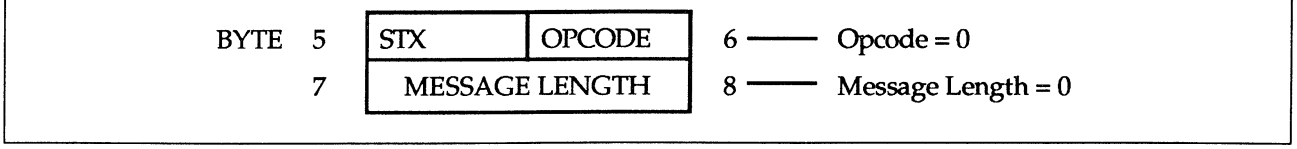
ATTENTION This instruction is executed only when the DCM has placed the 620 CPM in the software PROGRAM mode. The DCM program memory write protect function must be disabled to execute this instruction.

Figure 5-77 Download Title Instruction Format



ATTENTION Data must be encoded in ASCII. Byte 9 contains the first character of the statement. Unused bytes should be loaded with space characters (ASCII 20).

Figure 5-78 Download Title Response Format (Instruction Executed)



Diagnostic Instructions

Purpose

These instructions obtain DCM and 620 CPM status information and ensure that the physical data link between the host and the DCM is functioning properly.

Continued on next page

Read DCM status

This instruction is a diagnostic tool for the host computer. It obtains DCM and processor status information and provides a tabulation of message exchanges that have occurred since DCM power initialization or since the last Read DCM Status instruction. Message exchange counters are reset during execution of the Read DCM Status instruction. Refer to Figure 5-79 for the instruction format and Figure 5-80 for the response format for this instruction.

Figure 5-79 Read DCM Status Instruction Format

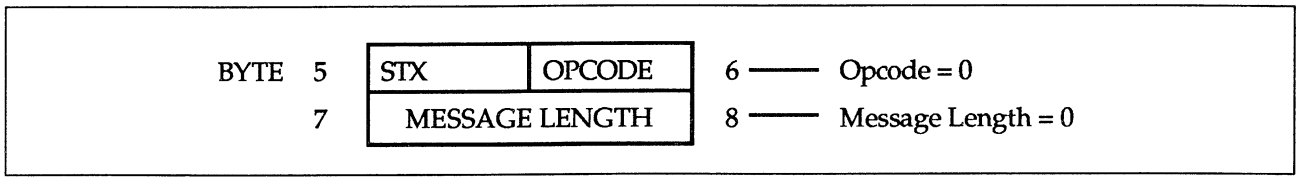
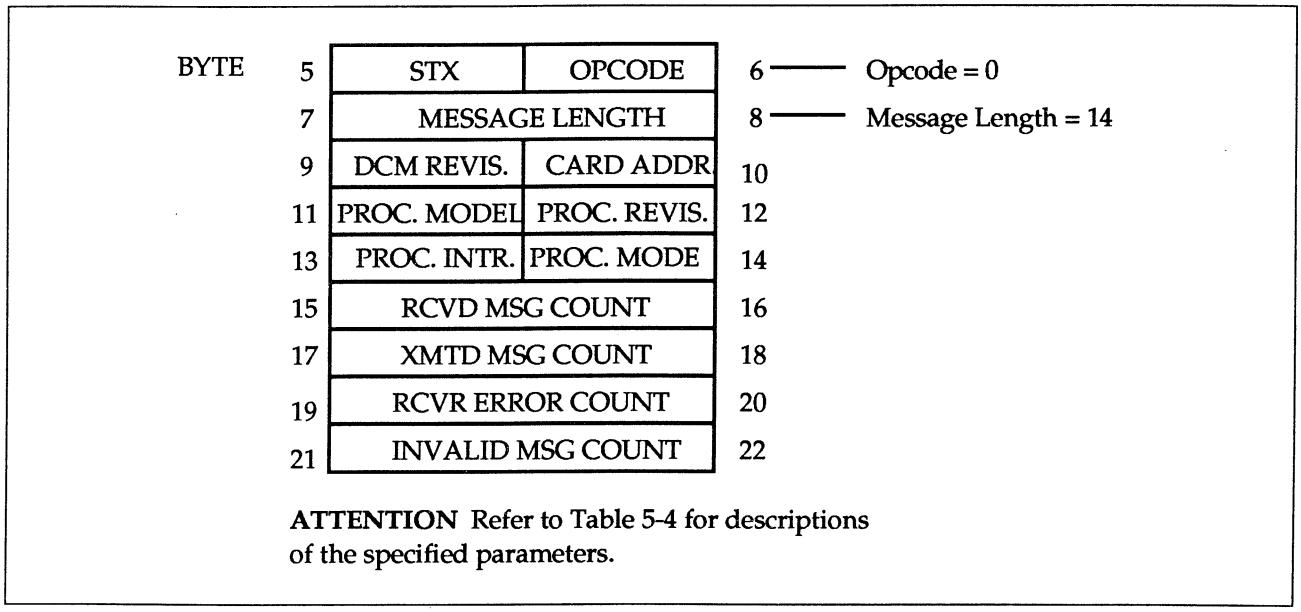


Figure 5-80 Read DCM Status Response Format (Instruction Executed)



ATTENTION Refer to Table 5-4 for descriptions of the specified parameters.

Continued on next page

Read DCM status,
continued

Table 5-4 Descriptions for Read DCM Status Response Parameters

Item	Description
DCM Revision	A binary number that represents the DCM revision level.
Card Address	A binary number from 0 to 3 that represents the address of the DCM on the 620 CPM backplane.
Processor Model	A binary number representing the 620 CPM as follows: 1 = 620-06 1 = 620-1631 0 = 620-10 1 = 620-1633 1 = 620-11 2 = 620-20 1 = 620-12 3 = 620-25 1 = 620-14 3 = 620-30 1 = 620-15 3 = 620-35 1 = 620-36
Processor Revision	Extracted from the processor revision byte in the processor System Status Table.
Processor Interface	A representation of the state of the DCM/processor interface as follows: 0 = not yet established, or no longer responsive 1 = functional
Processor Mode	A representation of the general state of the processor as follows: 0 = PROGRAM mode 1 = RUN mode (includes DISABLE and RUN/PROGRAM modes)
Received Message Counter	A 16-bit binary count of the number of messages received successfully since the last Read DC M Status instruction or since DCM power initialization.
Transmitted Message Counter	A 16-bit binary count of the number of messages transmitted by the DCM since power initialization or since the last Read DCM Status instruction.
Receiver Error Count	A 16-bit binary count of the number of receiver errors, which may be checksum errors or message header errors. This count can be incremented only if an SOH followed by a valid nodal address have first been received. The counter is reset at power initialization or following the formulation of a Read DCM Status response. Message aborts are not considered receiver errors.
Invalid Message Counter	A 16-bit binary count of the number of messages received that contain invalid opcodes, control characters, and modifiers. The counter is reset at power initialization or following the formulation of a Read DCM Status response.
Execution Time	The DCM will have a response ready for transmission within 1 ms of receiving this command, unless the DCM is processing a previous instruction or a processor command.

Continued on next page

Loop back test

This instruction is a diagnostic tool for the host computer. It echoes a test message sent by the host that aids in data link diagnostics. If the DCM does not receive the proper host data, an invalid test response is sent. Refer to Figure 5-81 for the instruction format and Figure 5-82 for the response format for this instruction.

Figure 5-81 Loop Back Test Instruction Format

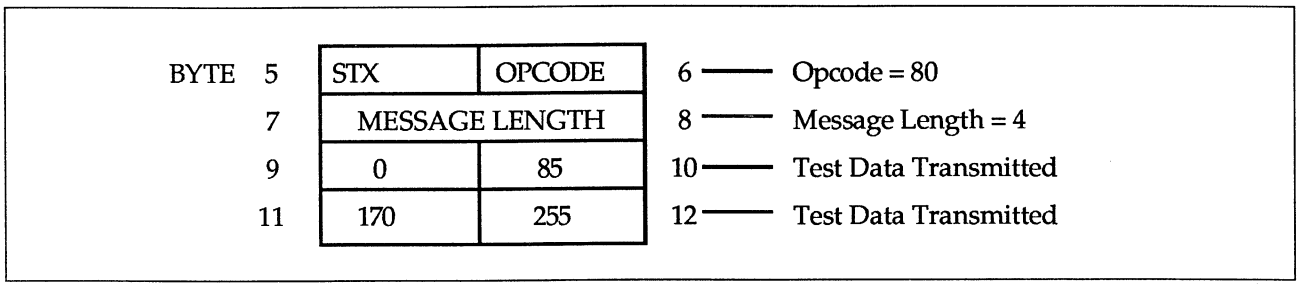
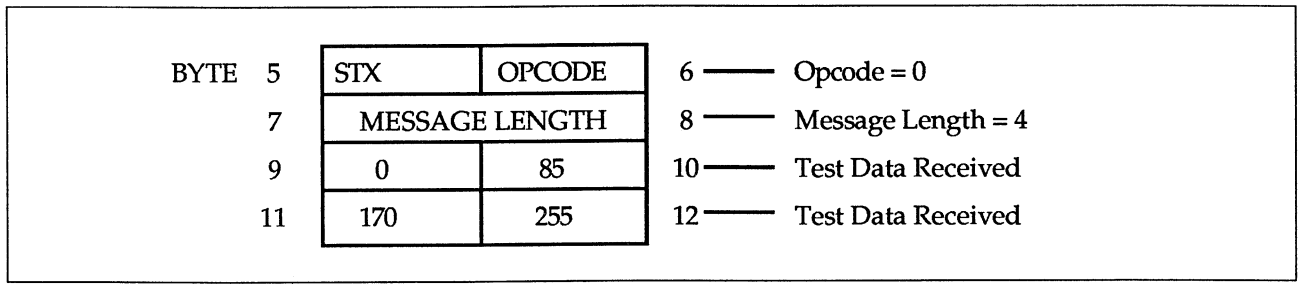


Figure 5-82 Loop Back Test Response Format (Instruction Received, Data Verified)



Instruction Execution Times

Approximate instruction execution times in milliseconds

Refer to Table 5-5 for instruction execution times for the various 620 CPMs used with the 620-0048/620-0052 DCM.

Table 5-5 Approximate Instruction Execution Times (in Milliseconds)

Instruction	620-06/10/15	620-11/14/1631	620-12/1633/36	620-20/25/30/35
Input/Output Instructions				
Read 16N I/O	0.24 + N(0.210)	0.040 + N(.149)	0.040 + N(0.123)	0.14 + N(0.039) [1]
Read 16N Scattered I/O	0.26 + N(0.208)	0.013 + N(.179)	0.013 + N(0.153)	0.14 + N(0.043)
Write N Outputs	0.40 + N(0.014)	0.259 + N(.018)	0.259 + N(0.019)	0.22 + N(0.006) [2]
Write 16N Outputs	0.26 + N(0.207)	0.074 + N(.185)	0.074 + N(0.207)	0.17 + N(0.048) [3]
Write N Scattered Outputs	0.24 + N(0.131)	0.023 + N(.125)	0.023 + N(0.111)	0.13 + N(0.053)
Data Collection Instructions				
Initiate Data Collection	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Terminate Data Collection	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Read Data Buffer	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Read Mask Table	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Read Reference Table	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Write Mask Table	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Inhibit Mask Table	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Enable Mask Table	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Register Instructions				
Read N Registers, No Sign	0.23 + N(0.132)	0.074 + N(.127)	0.074 + N(0.112)	0.12 + N(0.035)
Read N Signed Registers	0.38 + N(0.157)	0.074 + N(.127)	0.074 + N(0.112)	0.28 + N(0.060)
Read N Scattered Registers	0.24 + N(0.131)	0.030 + N(.129)	0.030 + N(0.114)	0.13 + N(0.040)
Write N Registers, No Sign	0.24 + N(0.132)	0.074 + N(.127)	0.074 + N(0.112)	0.17 + N(0.036)
Write N Signed Registers	0.28 + N(0.132)	0.074 + N(.127)	0.074 + N(0.112)	0.14 + N(0.060)
Write N Scattered Registers	0.25 + N(0.132)	0.027 + N(.147)	0.027 + N(0.132)	0.13 + N(0.037)
Pull N I/O Registers	0.43 + N(0.156)	0.281 + N(.179)	0.281 + N(0.172)	0.17 + N(0.053)
Push N I/O Registers	0.41 + N(0.156)	0.040 + N(.311)	0.040 + N(0.304)	0.21 + N(0.049)
Read N System Status Registers	0.35 + N(0.183)	0.100 + N(.245)	0.100 + N(0.233)	0.14 + N(0.083)
Write N System Status Registers		0.070 + N(.122)	0.070 + N(0.107)	
620 LCS Processor Control Instructions				
Request PROGRAM Mode[4]				
Remove PROGRAM Mode Request[5]				
Write I/O Configuration		0.296 + N(.121)	0.267 + N(0.106)	
Write Processor Control Configuration		0.538	0.493	

1. Exchange Time = 0.15 + N(0.413) above address 4095 in 620-20/25 and 620-30/35 processors only.
2. Exchange Time = 0.22 + N(0.028) above address 4095 in 620-20/25 and 620-30/35 processors only.
3. Exchange Time = 0.16 + N(0.433) above address 4095 in 620-20/25 and 620-30/35 processors only.
4. Refer to Table 5-6 for calculation procedure for the Request PROGRAM Mode execution time.
5. Refer to Table 5-7 for calculation procedure for the Remove PROGRAM Mode Request execution time.

Continued on next page

Approximate instruction execution times in milliseconds, continued

Table 5-5 Approximate Instruction Execution Times (in Milliseconds), Continued

Instruction	620-06/10/15	620-11/14/1631	620-12/1633/36	620-20/25/30/35
Program Memory Instructions				
Upload N Program Memory Words	0.36 + N(0.174)	0.402 + N(.168)	0.383 + N(0.140)	0.15 + N(0.038)
Download N Program Memory Words[6]				
Clear Program Memory	120.6	577	347	82
Insert N Program Memory Words[7]				
Delete N Program Memory Words[8]				
Program Header Instructions				
Upload Program Date	1.1	0.772	0.696	0.4
Upload Programmer	4.0	3.150	2.820	1.2
Upload Title	14.0	11.560	10.341	4.1
Download Program Date	1.1	0.772	0.683	0.4
Download Programmer	3.8	3.150	2.765	1.1
Download Title	13.6	11.520	10.099	3.8
Diagnostic Instructions				
Read DCM Status[9]	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0
Loop Back Test	approx. 1.0	approx. 1.0	approx. 1.0	approx. 1.0

6. Refer to Tables 5-8 and 5-9 for calculation procedure for the Download N Program Memory Words execution time.
7. Refer to Tables 5-10 and 5-11 for calculation procedure for the Insert N Program Memory Words execution time.
8. Refer to Tables 5-12 and 5-13 for calculation procedure for the Delete N Program Memory Words execution time.
9. The DCM has a response ready for transmission within 1ms of receiving this command, unless the DCM is processing either a previous instruction or a processor command.

Continued on next page

Approximate instruction execution times in milliseconds, continued

Table 5-6 Request PROGRAM Mode Execution Time

CPM	Processor in RUN Mode, Switched to PROGRAM Mode	Processor Already in PROGRAM Mode
620-06/10/15	Time (ms) = 4.8 + Irregular Processor Overhead*	Time (ms) = 1.2 + Irregular Processor Overhead*
620-11/14/1631	Time (ms) = 5.2 + Irregular Processor Overhead*	
620-12/1633/36	Time (ms) = 5.2 + Irregular Processor Overhead*	
620-20/25/30/35	Time (ms) = 3.6 + Irregular Processor Overhead*	Time (ms) = 1.3 + Irregular Processor Overhead*

* Time incurred in response to external stimuli such as communication with a Loader/Terminal or other communication interface modules.

Table 5-7 Remove PROGRAM Mode Request Execution Time

CPM	Processor in PROGRAM Mode, Switched to RUN Mode	Processor in PROGRAM Mode Stays in PROGRAM Mode Because of Another Mode Control Input
620-06/10/15	Time (ms) = 480 + Irregular Processor Overhead*	Time (ms) = 1.2 + Irregular Processor Overhead*
620-11/14/1631	Time (ms) = 792 + Irregular Processor Overhead*	Time (ms) = 1.2 + Irregular Processor Overhead*
620-12/1633/36	Time(ms) = 725 + Irregular Processor Overhead*	Time (ms) = 1.2 + Irregular Processor Overhead*
620-20/25/30/35	Time (ms) = 660 + Irregular Processor Overhead*	Time (ms) = 1.3 + Irregular Processor Overhead*

* Time incurred in response to external stimuli such as communication with a Loader/Terminal or other communication interface modules.

Continued on next page

Approximate instruction execution times in milliseconds, continued

Table 5-8 Download N PROGRAM Memory Words Execution Time†

CPM	Execution Time
620-06/10/15	$T_R + T_W + T_F + T_D$
620-11/14/1631	$T_R + T_W + T_F + T_D$
620-12/1633/36	$T_R + T_W + T_F + T_D$
620-20/25/30/35	$T_R + T_W + T_F + T_D$

† Refer to Table 5-8 (below) for Insert PROGRAM Memory Words execution time calculation parameters.

T_R = time to read processor memory to be overwritten.

T_W = time until processor cycles through its normal overhead and provides another window.

T_F = time to search processor memory to be overwritten to check for forced opcodes.

T_D = time to download N program memory words.

Table 5-9 Download N PROGRAM Memory Words Execution Time Calculation Parameters

	Time (milliseconds)			
Parameter	**620-06/10/15**	**620-11/14/1631**	**620-12/1633/36**	**620-20/25/30/35**
T_R	0.36 + N(0.174)	0.36 + N(0.174)	0.341 + N(0.146)	0.15 + N(0.038)
T_W	1.2 + Irregular Overhead*	2.4 + Irregular Overhead*	2.4 + Irregular Overhead*	1.7 + Irregular Overhead*
T_F	0.019 + N(0.118)	0.019 + N(0.118)	0.019 + N(0.118)	0.019 + N(0.118)
T_D	0.94 + N(0.221)	1.60 + N(0.210)	1.581 + N(0.281)	0.34 + N(0.057)

* If the program is downloading while the processor is in the RUN mode, T_W = processor scan time.

Continued on next page

Approximate instruction execution times in milliseconds, continued

Table 5-10 Insert N PROGRAM Memory Words Execution Time†

CPM	Execution Time
620-06/10/15	$T_O + T_W + T_I + T_F$
620-11/14/1631	$T_O + T_W + T_I + T_F$
620-12/1633/36	$T_O + T_W + T_I + T_F$
620-20/25/30/35	$T_O + T_W + T_I + T_F$

† Refer to Table 5-10 (below) for Insert N PROGRAM Memory Words execution time calculation parameters.

T_O = time to open gap in user memory.

T_W = time until processor cycles through its normal overhead and provides another window.

T_I = time to insert the desired memory.

T_F = time to search processor memory to be overwritten to check for forced opcodes.

M = number of user memory words from starting address to end of program.

Table 5-11 Insert N PROGRAM Memory Words Execution Time Calculation Parameters

	Time (milliseconds)			
Parameter	**620-06/10/15**	**620-11/14/1631**	**620-12/1633/36**	**620-20/25/30/35**
T_O	1.35 + M(0.054)	1.0 M(0.035)	0.813 + M(0.034)	0.45 + M(0.045)
T_W	1.20 + Irregular Overhead*	2.40 + Irregular Overhead*	2.40 + Irregular Overhead*	1.70 + Irregular Overhead*
T_I	1.27 + M(0.221)	1.50 + M(0.20)	1.481 + N(0.271)	0.44 + M(0.056)
T_F	0.017 + M(0.059)	0.017 + M(0.059)	0.017 + M(0.059)	0.017 + M(0.059)

* Time incurred in response to external stimuli such as communication with a Loader/Terminal or other communication interface modules.

Continued on next page

Approximate instruction execution times in milliseconds, continued

Table 5-12 Delete N PROGRAM Memory Words Execution Time†

CPM	Execution Time
620-06/10/15	$T_R + N/150 + T_W + T_F + T_D$
620-11/14/1631	$T_R + N/150 + T_W + T_F + T_D$
620-12/1633/36	$T_R + N/150 + T_W + T_F + T_D$
620-20/25/30/35	$T_R + N/150 + T_W + T_F + T_D$

† Refer to Table 5-12 (below) for Delete N PROGRAM Memory Words execution time calculation parameters.

T_R = time to read processor memory to be overwritten.

T_W = time until processor cycles through its normal overhead and provides another window.

T_F = time to search processor memory to be overwritten to check for forced opcodes.

T_D = time to delete N program memory words.

Table 5-13 Delete N PROGRAM Memory Words Execution Time

	Time (milliseconds)			
Parameter	620-06/10/15	620-11/14/1631	620-12/1633/36	620-20/25/30/35
T_R	0.36 + N(0.174)	0.36 + N(0.174)	0.341 + N(0.146)	0.15 + N(0.038)
T_W	1.2 + Irregular Overhead*	2.4 + Irregular Overhead*	2.4 + Irregular Overhead*	1.7 + Irregular Overhead*
T_F	0.008 + N(0.065)	0.008 + N(0.065)	0.008 + N(0.065)	0.008 + N(0.065)
T_D	1.35 + N(0.054)	0.56 + N(0.0033)	0.439 + N(0.0024)	0.66 + N(0.045)

* Time incurred in response to external stimuli such as communication with a Loader/Terminal or other communication interface modules.

Flag Mode Operation Response

DCM Flag Mode Response Function

This response is generated if an OFF to ON change has occurred. Various methods of energizing flag outputs are available to the processor programmer. The flag outputs in the 620 LCS program memory should be latch outputs to ensure that all flag responses are transmitted to the host. The host's application program should indicate that it has received the flag response by resetting these latch outputs (that is, turning them OFF).

Refer to Table 5-14 for flag bits for each of the 620 Logic Controller Systems:

Table 5-14 Flag Bits for 620 Logic Controller Systems

620 LCS	Flag Bit Locations
620-06/10/15	752 to767
620-11/14/1631 †	2016 to 2031
620-12/1633/36	2016 to 2031
620-20/25/30/35	2032 to 2047

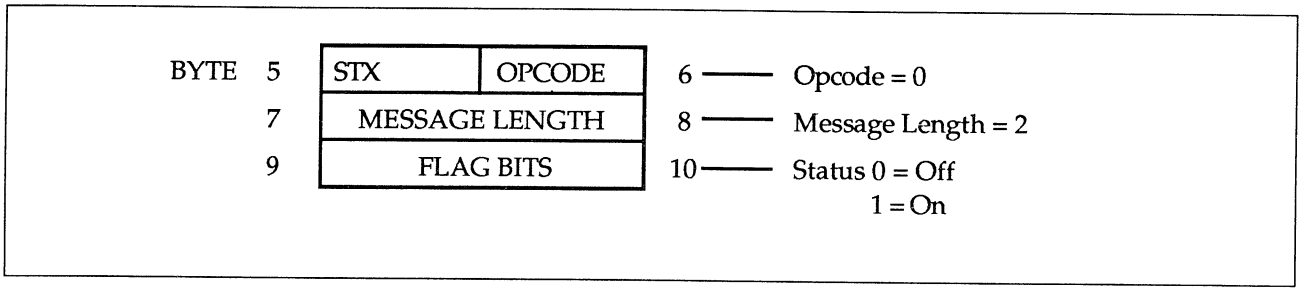
† Flag bit location is programmable in the 620-11/14/1631 LCS; the values listed for the 620-11/14/1631 are default values.

Flag responses are generated automatically when a transition occurs. The flag bits are read at every processor backplane window if the flag mode is enabled and the DCM is not receiving a message or servicing a command. Flag bits are packed into a 16-bit message. The least significant bit of the data is the content of the least significant flag address.

The DCM flag mode response function must be enabled and the point-to-point serial port configuration must be selected to execute this function. The flag mode is disabled if the port is in data collection mode. The control character equals 132.

Refer to Figure 5-83 for the DCM Flag Mode Response Function.

Figure 5-83 DCM Flag Mode Response Function



Error Messages

Error messages and opcodes

A response occurs in most host/DCM exchanges. This response can be either an acknowledge or an error message. Refer to Table 5-15 for a listing of the possible error messages and their respective opcodes. Descriptions of the error messages and conditions under which they are generated are presented throughout the remainder of this section.

Table 5-15 Error Messages and Opcodes

OPCODE	ERROR MESSAGE
1	Invalid Opcode
2	N Value Exceeds System Limits
3	Starting Address Exceeds Memory Limits
4	Memory Block Exceeds Memory Limits
5	Invalid Processor Mode (see ATTENTION below)
6	User Program Memory Not Alterable (ROM)
7	Write Protect Enabled
8	Data Collection in Progress
9	Reference Table Not Initialized
17	Processor Access Denied
80	Invalid Loop Back Test

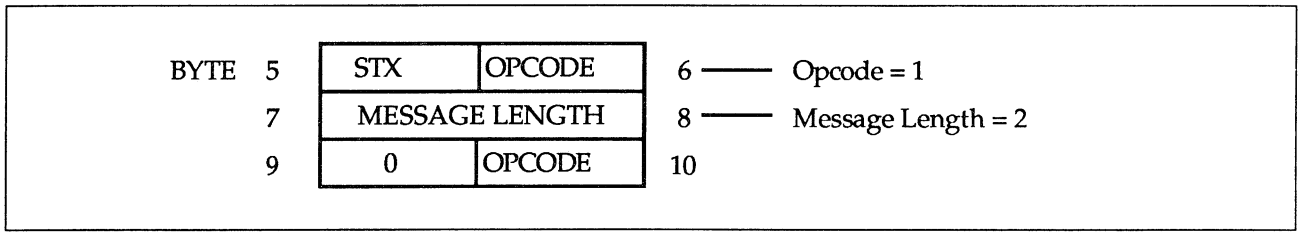
ATTENTION Opcode 5 – Invalid Processor Mode will occur if the 620-0048/0052 DCM attempts to write to a processor's program memory while Augmented Run Mode Programming is in progress. It is impossible to execute the write command if the Loader/Terminal is in ARMP.

Continued on next page

Invalid Opcode

This response occurs when the DCM receives an opcode for which it has no service routine. The invalid opcode is returned in the least significant byte (byte 10) of a data word included with the message. Refer to Figure 5-84 for the response format for this error message.

Figure 5-84 Invalid Opcode Response Format (Error Message)

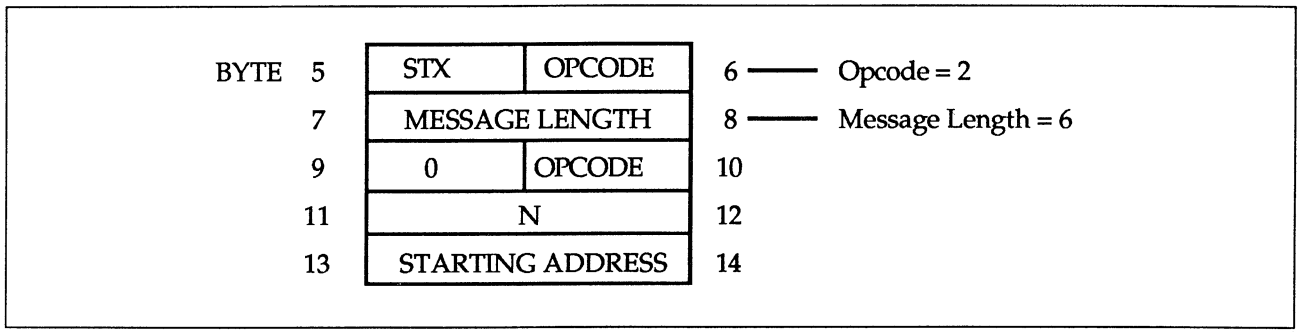


Continued on next page

N Value Exceeds System Limits

This response indicates that the N value in the instruction exceeds the system limits. The invalid N value as well as the instruction opcode are returned with the message. The starting address is included for error message consistency. Refer to Figure 5-85 for the response format for this error message.

Figure 5-85 N Value Exceeds System Limits Response Format (Error Message)

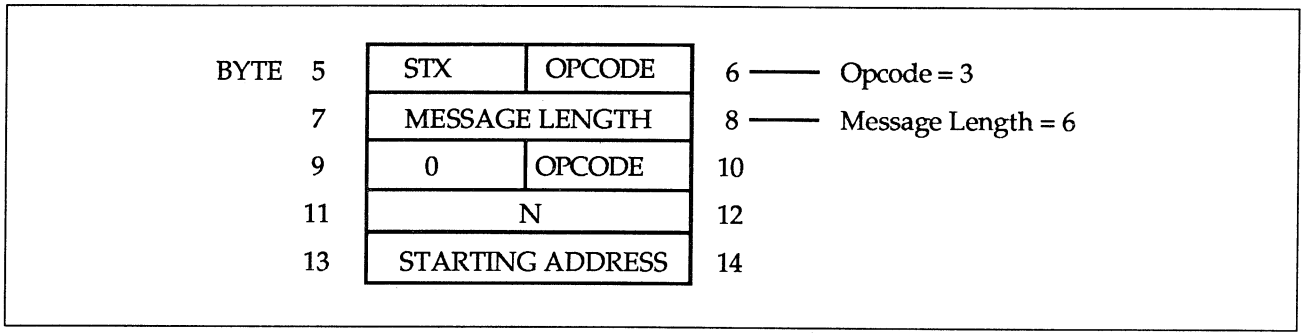


Continued on next page

Starting Address Exceeds Memory Limits

This response indicates that the starting address value in the instruction exceeds the system limits. The invalid starting address, N value, and opcode are returned with the error message. Refer to Figure 5-86 for the response format for this error message.

Figure 5-86 Starting Address Exceeds Memory Limits Response Format (Error Message)

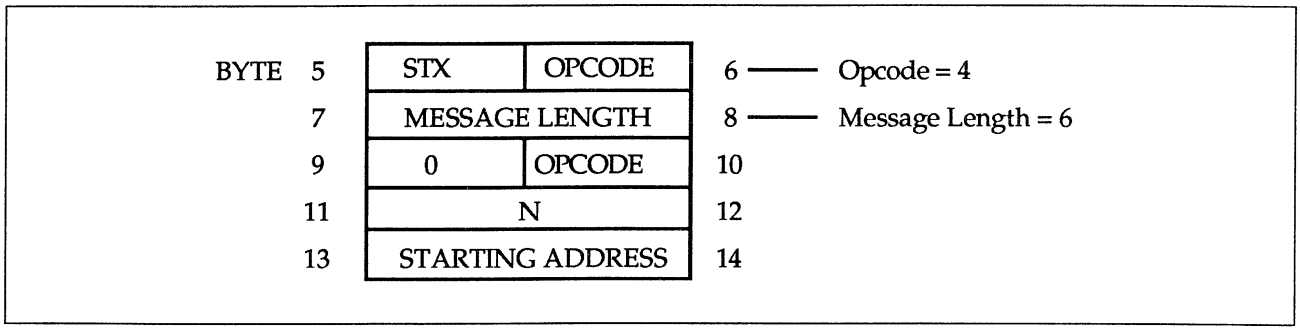


Continued on next page

Memory Block Exceeds Memory Limits

This response indicates that the defined memory block does not fall within the bounds of the 620 LCS processor memory for situations where the N value and starting address are valid but the memory block they define is not. The error opcode, the instruction opcode, the N value, and the starting address are returned (the starting address and N value define a block of memory for the instruction opcode). Refer to Figure 5-87 for the response format for this error message.

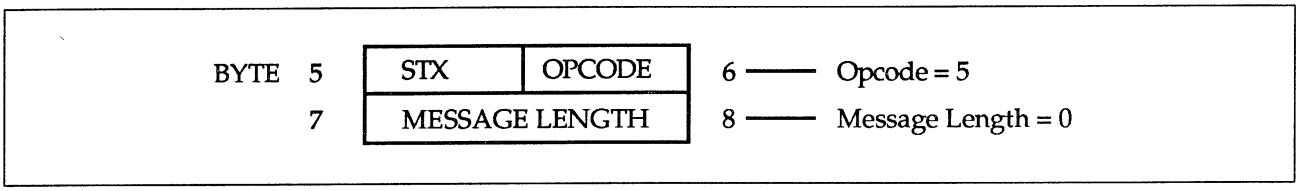
Figure 5-87 Memory Block Exceeds Memory Limits Response Format (Error Message)



Continued on next page

Invalid Processor Mode This response occurs when the mode check fails prior to instruction execution. The response applies only to the program memory status table and PUSH/PULL instructions. Refer to Figure 5-88 for the response format for this error message.

Figure 5-88 Invalid Processor Mode Response Format (Error Message)



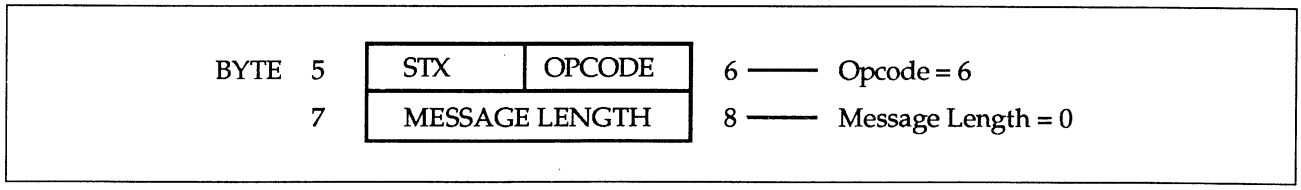
ATTENTION This response will occur if the 620-0048/0052 attempts to write to a processor's program memory while Augmented Run Mode Programming is in progress. It is impossible to execute the write command if the Loader/Terminal is in ARMP.

Continued on next page

User Program Memory Not Alterable

This response occurs with instructions that attempt to write to program memory when that memory is in ROM. Refer to Figure 5-89 for the response format for this error message.

Figure 5-89 User Program Memory Not Alterable Response Format (Error Message)

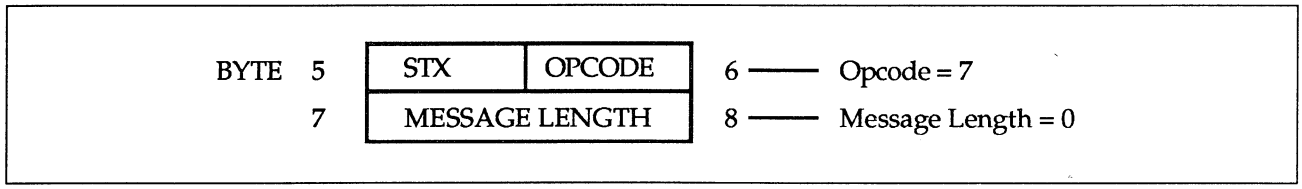


Continued on next page

Write Protect Enabled

This response occurs with write instructions that are directed to a memory that has its write protect function enabled. Refer to Figure 5-90 for the response format for this error message.

Figure 5-90 Write Protect Enabled Response Format (Error Message)

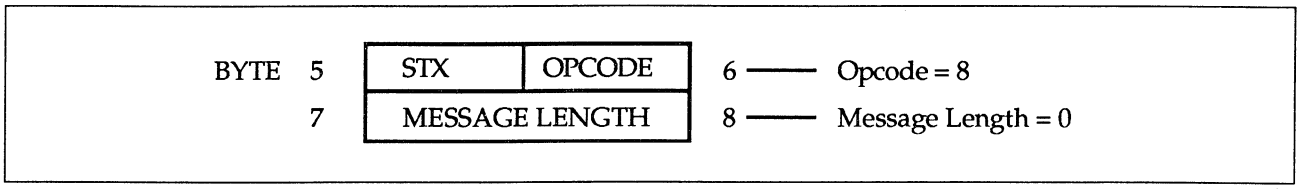


Continued on next page

Data Collection in Progress

This response occurs if the DCM receives a Read Reference Table or Write Mask Table instruction while the DCM is in the data collection mode. Refer to Figure 5-91 for the response format for this error message.

Figure 5-91 Data Collection in Progress Response Format (Error Message)

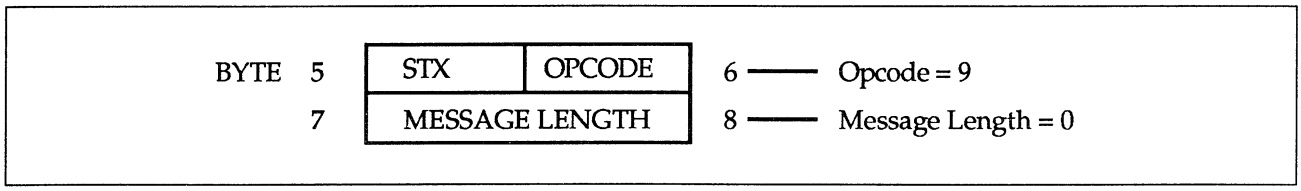


Continued on next page

Reference Table Not Initialized

This response occurs if the Read Reference Table instruction is attempted before the referenced table is initialized. The DCM must enter the data collection mode to initialize the table and must exit the data collection mode before the reference table can be read. Refer to Figure 5-92 for the response format for this error message.

Figure 5-92 Reference Table Not Initialized Response Format (Error Message)

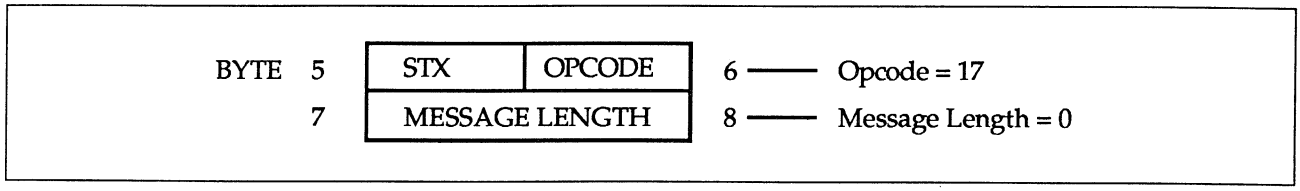


Continued on next page

Processor Access Denied

The DCM receives limited control of the processor during the Memory Word Zero portion of processor operation. During this window, the DCM exchanges data with the processor. The DCM assumes it is no longer recognized by the processor if this window fails to open within approximately 7 seconds (worst case scan time plus). If this occurs, any instructions to the DCM that require data exchanges with the processors result in a Processor Access Denied error message. Refer to Figure 5-93 for the response format for this error message.

Figure 5-93 Processor Access Denied Response Format (Error Message)

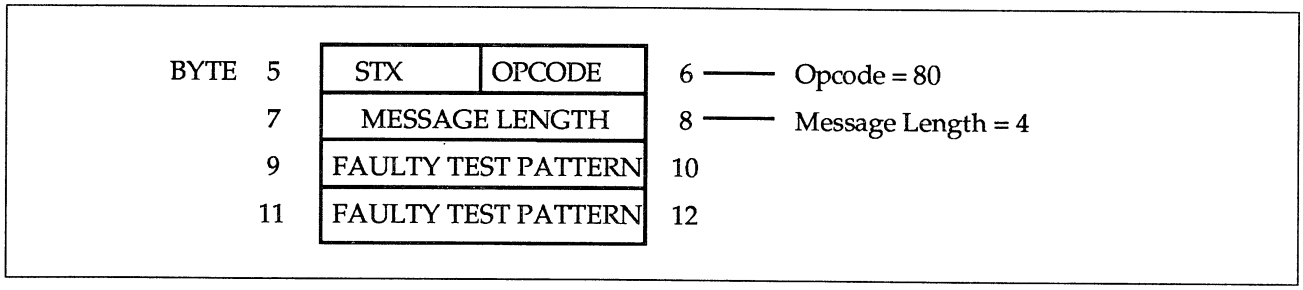


Continued on next page

Invalid Loop Back Test

This response occurs if an error has occurred in the Loop Back Test. The faulty test pattern received is returned in the message. Refer to Figure 5-94 for the response message for this error message.

Figure 5-94 Invalid Loop Back Test Response Format (Error Message)



Appendix

Overview

Appendix contents

Instruction set opcodes Refer to Table A-1 for 620-0048/0052 DCM opcode instructions in decimal "byte" form and single bit form. Associated with opcodes are 16 bits of address or associated data expressed as two-byte values in decimal form. The comma separating the values is not used in programming.

ASCII conversion Refer to Table A-2 for ASCII-to-decimal conversions.

DCM Instruction Set Opcodes

Table A-1 DCM Instruction Set Opcodes

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21[1]	20[1]	19	18	17	16	15 - - - - - - - - - - - - - - - 0
Input Status Scan	8F	1	0	D	F	1	1	1	1	32767 Dec./7FFF Hex.[2]
No Operation	FF	1	1	1	1	1	1	1	1	32767 Dec./7FFF Hex.[2]
Bit Read	03	0	0	0	0	0	0	1	1	Hex. Address
Normally Open Contact										
No Packed Down Branches	C8	1	1	D	F	1	0	0	0	Address
One Packed Down Branch	C9	1	1	D	F	1	0	0	1	Address
Two Packed Down Branches	CA	1	1	D	F	1	0	1	0	Address
Normally Closed Contact										
No Packed Down Branches	CC	1	1	D	F	1	1	0	0	Address
One Packed Down Branch	CD	1	1	D	F	1	1	0	1	Address
Two Packed Down Branches	CE	1	1	D	F	1	1	1	0	Address
Not	CB	1	1	0	0	1	0	1	1	Address
Transition ON Contact	43	0	1	D	F	0	0	1	1	Address[3]
Transition OFF Contact	4B	0	1	D	F	1	0	1	1	Address[3]
Branch (three internal instructions)										
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Double-Down Branch	C2	1	1	0	0	0	0	1	0	Not Used
Up Branch	C3	1	1	0	0	0	0	1	1	32767 Dec./7FFF Hex.[2]
Output	C4	1	1	D	F	0	1	0	0	Address
Retentive Output	C5	1	1	D	F	0	1	0	1	Address
Latch Output	C6	1	1	D	F	0	1	1	0	Address
Unlatch Output	C7	1	1	D	F	0	1	1	1	Address
Bit Write	85	1	0	D	F	0	1	0	1	Address
F. P. Constant in LS Register	9B	1	0	0	1	1	0	1	1	Address
F. P. Constant in MS Register	AB	1	0	1	0	1	0	1	1	Address
F. P. Bring In	A8	1	0	1	0	1	0	0	0	Address
F.P. Send Out	27	0	0	1	0	0	1	1	1	Address
Bring In	88	1	0	0	0	1	0	0	0	Address
Send Out	7	0	0	D	F	0	1	1	1	Address[4]
Constant	8B	1	0	0	0	1	0	1	1	Data
Indirect Bring In	89	1	0	0	0	1	0	0	1	Address
Indirect Send Out	06	0	0	0	0	0	1	1	0	Address
Pull from I/O	80	1	0	0	0	0	0	0	0	Registers[5] Address
Pull from Status Table	81	1	0	0	0	0	0	0	1	Registers[5] Offset[6]
Pull from Registers	82	1	0	0	0	0	0	1	0	Registers[5] Offset[6]
Push to I/O	84	1	0	0	0	0	1	0	0	Registers[5] Address
Push to Registers	86	1	0	0	0	0	1	1	0	Registers[5] Offset[6]
End Of Memory	30	0	0	1	1	0	0	0	0	32768 Dec./8000 Hex.[2]
Not Skip and Retain	46	0	1	D	F	0	1	1	0	0 - 0, label
Not Skip and Deenergize	47	0	1	D	F	0	1	1	1	0 - 0, label[7]
End of Skip	34	0	0	1	1	0	1	0	0	0 - 0, label
Jump	46	0	1	D	F	0	1	1	0	0 - 0, label[8]
Return to Beg. of Program	5	0	0	D	F	0	1	0	1	32767 Dec./7FFF Hex.[2]
Delay	CF	1	1	0	0	1	1	1	1	Address

Notes begin at the end of the table.

Continued on next page

Table A-1 DCM Instruction Set Opcodes, continued

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21[1]	20[1]	19	18	17	16	15 ----------
On Delay Timer										
Word 1: (.01 sec.)	68	0	1	H	0	1	0	0	0	Address of elapsed time[7]
(.1 sec.)	69	0	1	H	0	1	0	0	1	Address of elapsed time[7]
(1 sec.)	6A	0	1	H	0	1	0	1	0	Address of elapsed time[7]
Word 2	C4	1	1	D	F	0	1	0	0	Output Address
Off Delay Timer										
Word 1: (.01 sec.)	60	0	1	H	0	0	0	0	0	Address of elapsed time[9]
(.1 sec.)	61	0	1	H	0	0	0	0	1	Address of elapsed time[9]
(1 sec.)	62	0	1	H	0	0	0	1	0	Address of elapsed time[9]
Word 2	C4	1	1	D	F	0	1	0	0	Output Address
Retentive On Delay Timer										
(.01 sec.)	4C	1	1	H	0	1	1	0	0	Address of elapsed time[9]
(.1 sec.)	6D	0	1	H	0	1	1	0	1	Address of elapsed time[9]
(1 sec.)	6E	0	1	H	0	1	1	1	0	Address of elapsed time[9]
Up/Down Counter	4F	0	1	H	H	1	1	1	1	Addr. - Accumulated Count [9]
Sequencer										
Sequencer Size	8A	1	0	0	0	1	0	1	0	Total # of Step(s)[10]
Step Number Address	8C	1	0	0	0	1	1	0	0	Address
Data Table Step 1	8B	1	0	0	0	1	0	1	1	Data
Control Output Address	07	0	0	0	0	0	1	1	1	Control Output Address
Load Sequencer	44	0	1	0	0	0	1	0	0	Address
Unload Sequencer	45	0	1	0	0	0	1	0	1	Address
Jump to Subroutine (JSR)										
Word 1	04	0	0	0	0	0	1	0	0	Address of zero (MAR)
Word 2	04	0	0	0	0	0	1	0	0	128, Label[11]
Subroutine (SUB)	24	0	0	1	0	0	1	0	0	128, Label[11]
Return to Subroutine (RTS)	14	0	0	0	1	0	1	0	0	128, Label[11]
BCD-BIN Conversion	0F	0	0	0	0	1	1	1	1	Address
BIN-BCD Conversion	1F	0	0	0	1	1	1	1	1	Address
F. P. to Integer Conversion	3F	0	0	1	1	1	1	1	1	Address
Integer to F. P. Conversion	2F	0	0	1	0	1	1	1	1	Address
AND	2C	0	0	1	0	1	1	0	0	Address
OR	2E	0	0	1	0	1	1	1	0	Address
Exclusive OR	3E	0	0	1	1	1	1	1	0	Address
Absolute Value	1C	0	0	0	1	1	1	0	0	Address
F. P. Square Root	2D	0	0	1	0	1	1	0	1	Address
Invert (1's Complement)	1D	0	0	0	1	1	1	0	0	Address
Negate (2's Complement)	1E	0	0	0	1	1	1	1	0	Address
Addition	0E	0	0	0	0	1	1	1	0	32767 Dec./7FFF Hex.[2]
Subtraction	0D	0	0	0	0	1	1	0	1	32767 Dec./7FFF Hex.[2]
Multiplication	0C	0	0	0	0	1	1	0	0	32767 Dec./7FFF Hex.[2]
Division	0B	0	0	0	0	1	0	1	1	32767 Dec./7FFF Hex.[2]
Equality Comparison	08	0	0	0	0	1	0	0	0	32767 Dec./7FFF Hex.[2]
Less Than Comparison	09	0	0	0	0	1	0	0	1	32767 Dec./7FFF Hex.[2]
Greater Than Comparison	0A	0	0	0	0	1	0	1	0	32767 Dec./7FFF Hex.[2]
Test for Zero	8D	1	0	D	F	1	1	0	1	Address

Continued on next page

Table A-1 DCM Instruction Set Opcodes, continued

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21[1]	20[1]	19	18	17	16	15 - - - - - - - - - - - - - - - 0
Matrix (Sequenced by operation)										
MOVE, INVERT										
Enable Contact		Contact Opcode								
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Zero
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Operator
OR, AND, XOR										Address
Enable Contact		Contact Opcode								
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Address
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Operator
SET 0, SET 1										Address
Set 0 Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Set 1 Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Operator[12]
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address
Compare										
Address/Bit Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Operator[12, 13]
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address

Notes begin at the end of the table.

Continued on next page

Note 1

An F in bit 20 denotes a force bit that indicates if the force is ON or OFF. A D in bit 21 denotes a data bit that indicates the status of the force bit in the ON state. Note that a normally open contact has a power flow in the closed position while a normally closed contact has a power flow in the open position.

Status	Bit 20	Bit 21
1	FORCE	CLOSED
0	NO FORCE	OPEN

Note 2

Bits 0-15 contain the hex value 7FFF (32767 decimal) when not used by the instruction.

Note 3

Bit 21 indicates the status of the instruction from the previous scan when the FORCE (bit 20) is OFF. A "1" indicates that the instruction was ON from the previous scan.

Note 4

Bits 20 and 21 indicate the forced state of the send out. Both bits are set to 1 when the instruction is forced. The forced send out will be treated as a No Operation (NOP) on succeeding scans.

Note 5

Bits 13-15 contain a binary representation (x) where the value x + 1 is the number of registers to be used (0 = 1 register, 7 = 8 registers).

Note 6

Bits 0-12 contain a binary representation of the address offset for both PUSH and PULL instructions.

Status Table Address = Status Table Offset + 2048
Register Address = Register Offset + 4096

If Status Table Address ≤ 2047,
then Status Table Offset = Status Table Address + 2048

If Status Table Address > 2047 (max. value 4095)
then Status Table Offset = Status Table Address - 2048

Example:

```
2291          Instruction's Memory Word
[PUL]         1000 0001  0000 0000  1111 0011
  1             opcode     register      offset
offset = 243  Address: 243 + 2048 = 2291
```

Continued on next page

Note 7

Bit 20 is a history bit that indicates the state of the element on the previous scan. If it is set to 1, succeeding executions will be treated as a Skip and Retain.

Note 8

A Jump to EOS has a label within the range of 8192 to 8447. An Indirect Jump to an EOS has a label of 8448. A Jump to a program line has a label of 8449.

Note 9

An H in bit 21 is the time base history for timers and counters. A positive transition on bit 21 causes an increment of the count or time. A positive transition on bit 20 of the up/down counter causes a decrement of the count.

Note 10

Bits 0-15 contain a binary representation of the number of steps. Bits 11-15 contain zeroes.

Note 11

Bits 0-7 contain a binary representation of the label. Bits 8-15 contain a binary representation of 128 (80 hex).

Note 12

OPERATOR	DECIMAL EQUIVALENT
MOVE	0
INVERT	2
OR	4
AND	6
XOR	8
SET 0, SET 1	10
COMPARE	12

Note 13

Operators are located in bits 0-15.

ASCII-to-Decimal Conversion

Table for ASCII-to-decimal consversion

Table A-2 ASCII-to-Decimal Conversion

	0	1	2	3	4	5	6	7	8	9
0	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT
1	LF	VT	FF	CR	SO	SI	DLE	DC1	DC2	DC3
2	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS
3	RS	US	SP	!	"	#	$	%	&	'
4	(	)	*	+	,	-	.	/	0	1
5	2	3	4	5	6	7	8	9	:	;
6	<	=	>	?	@	A	B	C	D	E
7	F	G	H	I	J	K	L	M	N	O
8	P	Q	R	S	T	U	V	W	X	Y
9	Z	[	\	]	^	_	'	a	b	c
10	d	e	f	g	h	i	j	k	l	m
11	n	o	p	q	r	s	t	u	v	w
12	x	y	z	{	:	}	~	DEL		

Use of Table A-2

To use Table A-2:

1. Find the appropriate ASCII character on the table.
2. Read decimal equivalent from left to right.

Examples

The following are examples of how to use Table A-2:

A = 65
BEL = 07
x = 120

ATTENTION

ATTENTION: In the following descriptions, Data Terminal Equipment (DTE) refers to the DCM or host computer, and Data Communications Equipment (DCE) refers to a modem. The signal functional descriptions are applicable to both RS232 and RS422/RS485 signals.

Clear to Send (CTS, CS)

When the DCM is attached to a DCE, the Clear to Send Signal is generated by the DCE in response to the DCM Request to Send input. The signal indicates whether or not the DCE is ready to transmit. The DCM will not enter the transmit mode when Clear to Send is in the OFF condition.

The Clear to Send signal is not used between DTEs attached to one another. In this configuration, jumper the Clear to Send input to the Request to Send (RTS) output at each DCM's local attached connector. Jumpering this input to a fixed voltage (for example, +12V with RS232) also provides the ON condition. The definition of the RTS/CTS interchange requires the CTS to turn OFF before the RTS is asserted. Connecting the CTS to a fixed level does not satisfy this requirement.

Data Carrier Detect (DCD, RR)

When the DCM is attached to a DCE, the Data Carrier Detect input is controlled by the DCE. In the ON condition, the Data Carrier Detect indicates that the DCE is receiving a signal which meets its suitability criteria. In the OFF condition, the Data Carrier Detect indicates that no signal is being received or that the received signal is unsuitable for demodulation. When the DCD input is OFF, the DCM disables the receive mode.

The DCD input should be jumpered to its ON state when the DTE is attached to other DTEs or to a DCE that does not provide Data Carrier Detect. Jumper connections are made as follows:

Configuration	Jumper
RS232	20 to 8
RS422/RS485	19 to 24 7 to 23

Data Set Ready (DSR)

Signals on the Data Set Ready circuit indicate the status of an attached DCE. When this signal is OFF it indicates to the DCM that all other signals are to be disregarded. When the DCM is attached to another DTE or to a DCE that does not supply Data Set Ready, and when the DCM is operating in the RS232 configuration, the Data Set Ready input should be jumpered to its ON condition (pin 19 to pin 6).

Data Terminal Ready (DTR)

The Data Terminal Ready signal indicates to an attached DCE that the DCM is ready to operate in either the transmit or receive mode. This signal is ON whenever the processor in which the DCM is located is powered up and the asynchronous receiver/transmitter is functional.

Receive Data (RXD, RD)

Signals on the Receive Data Circuit are generated in response to data signals generated by the attached DCE via Receive Data, or by attached DTE via Transmit Data.

The Receive Data function is disabled under the following conditions:

1. Data Carrier Detect input is in the OFF condition.

2. In the half-duplex mode, Request to Send output is in the ON condition.

Both of these disabling functions are implemented via the DCM's executive firmware.

Request to Send (RTS, RS)

This circuit conditions the attached DCE for the transmit mode of the DTE. In the full-duplex mode, Request to Send has no internal control of the DTE transmitter or receiver. In the half-duplex mode, Request to Send has the following internal control functions:

1. When Request to Send is ON, the receive mode is disabled.
2. When operating in the RS422/RS485 configuration, Request to Send (OFF state) switches the Transmit Data line driver into the tristate mode (multidrop configuration only).

The attached DCE has the following control functions:

1. A transition of the DCM's RTS or RS signal from OFF to ON instructs the DCE to enter the transmit mode. After the DCE enters the transmit mode, it turns ON its Clear to Send circuit. The DCM will not enter the transmit mode until its Clear to Send input is ON.
2. A transition of the DCM's RTS or RS signal from ON to OFF instructs the DCE to complete the transmission of all data, to assume a nontransmit mode, and to remove the Clear to Send signal when the DCE is again prepared to receive another Request to Send input. Request to Send will not turn ON again until Clear to Send turns OFF.

The Request to Send function is not used between DTEs attached directly to one another. In this configuration, jumper the Request to Send output to its Clear to Send input on the local connector on each DTE.

Shield Ground

The shield ground input provides a direct connection to chassis ground. The cable shield is terminated at only one end in most applications.

Signal Ground

This conductor establishes the common ground reference potential for all RS232 interchange circuits except shield ground. This connection is not used in RS422/RS485 applications.

Transmit Data (TXD, SD)

Signals on this circuit are generated by the DCM for transmission of data to an attached DCE (into Transmit Data) or to an attached DTE (into Receive Data). The DCM holds Transmit Data in a marking condition during intervals between characters or words, and at all times when no data is being transmitted. The DCM transmits data only when an ON condition is present in all of the following circuits:

Request to Send
Clear to Send
Data Set Ready
Data Terminal Ready

Index

A, B

C

D

E

F

G, H

I, J, K

Continued on next page

L

M

N

O

P, Q

R, S

T

U, V

W, X, Y, Z

READER COMMENTS

Honeywell's IAC Automation College welcomes your comments and suggestions to improve future editions of this and other publications.

You can communicate your thoughts to us either by **mail** using this form, or a **toll-free telephone** call.

BY TELEPHONE: In the U.S.A. use our toll-free number 1*800-822-7673 (available in the 48 contiguous states except Arizona; in Arizona dial 1-602-863-5558).

BY MAIL: Use this form; detach, fold, tape closed, and mail to us. We would like to acknowledge your comments; please include your complete name and address.

Title of Publication: **620-0048 & 620-0052 Data Collection Modules User Manual**

Publication Number: **620-8980** Issue Date: **06/92**

Writer: **Doug Bonanomi**

COMMENTS: _____

_____

_____

_____

_____

_____

_____

_____

_____

RECOMMENDATIONS: _____

_____

_____

_____

_____

_____

_____

NAME _____ DATE _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

(If returning by mail, please tape closed; Postal regulations prohibit use of staples.)

Communications concerning technical publications should be directed to:

Automation College
Industrial Automation and Control
Honeywell Inc.
2820 West Kelton Lane
Phoenix, Arizona 85023

FOLD FOLD

From: _____

_____

_____

NO POSTAGE
NECESSARY
IF MAILED
IN THE USA

BUSINESS REPLY MAIL

FIRST CLASS **PERMIT NO. 4332** PHOENIX, ARIZONA

POSTAGE WILL BE PAID BY ....

Honeywell

Industrial Automation and Control
2820 West Kelton Lane
Phoenix, Arizona 85023

Attention: Manager, Quality

FOLD FOLD

Honeywell

Helping You Control Your World

Industrial Automation and Control
Honeywell, Inc.
1100 Virginia Drive
Fort Washington, Pennsylvania 19034